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## **A VLSI Framework for Parallel Long-Period Random Number Generator**

**R. Nageshwari and G .Sarala**

**Abstract :** Literature reported that hardware architecture for well-organized implementation of the reseeding method is not suitable for frame work analysis. Our aim achieves a throughput of one sample-per-cycle and runs on a Xilinx XC5VFX130T field-programmable gate array (FPGA) device. Accordingly the paper presents issues and challenges involved in above methods.