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### Low Frequency Noise Analysis in Twin Silicon

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Abstract - It has been observed from literature that because of the ability to effectively suppress off-leakage current with its gate-around configuration, the Si nanowire FET is considered to be the ultimate structure devices that would be approaching there downsized limits. Recently several experimental studies of Si nanowire FETs with on-currents much larger than those of planar MOSFETs have been published. Consequently, Si nanowire FET's are now gaining significant attention as the most promising candidate for mainstream CMOS devices in the 2020s. In this paper, the low frequency noise (LFN) in n-type silicon nanowire MOSFETs (SNWTs) is investigated for various gate lengths and various materials for improving drain current and reducing short channel effects. As a result, design optimization to reduce the impact of parasitic resistance in SNWTs are necessary for analog / RF applications.