Memory Protection In Arm Processor

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Abstract - Literature reported that the ARM processor core is a key component of many successful 32-bit embedded systems. Embedded systems often use multiple memory devices. The probability of having multiple errors is increased only when the size of memory increased. In order to maintain good level of reliability. It is necessary to protect memory cells from errors by protection codes. Error detection and correction (EDAC) codes plays a main role in memory protection and for reliability improvement. So, in this paper, an error detection and correction method to protect the memory against the errors is proposed. HHVD is high level error detection and correction method to protect against errors based on 4D parties checking for each row, column and diagonal in splash and black splash directions. It can correct up to 3 upsets in a data block but it can detect huge number of multiple faults in memories. It can improve the fault detection and correction coverage using parity codes which having low computation latency and implementation complexity.