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WCET Analysis on Real Time Embedded Systems

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Abstract: Literature review revealed that the growing density of integration and the increasing percentage of system on chip memory occupied by embedded programs have led to an increase in the expected amount of power consumption. In order to reduce the integrity and iterations of the embedded programs the WCET has been implemented. In this paper, a compiler level optimization, namely WCET aware rescheduling register allocation, is proposed to achieve WCET minimization for real time embedded systems. The novelty of the proposed approach is that the effects of register allocation, instruction scheduling, and cluster assignment on the quality of generated code are taken in to account for WCET minimization.