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# Design of 7T-SRAM for Nano Scale Technologies

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**Abstract**

On-chip store devours a huge level of the entire chip zone and expected to increment in trend setting innovations. Charging/releasing enormous piece lines capacitance speaks to a huge bit of intensity utilization during a compose activity. We propose a novel compose system which depends just on one of the no good lines to play out a compose activity. Hence, the proposed 7T SRAM cell decreases the movement factor of releasing the bitline pair to play out a compose activity. Test results utilizing HSPICE recreation demonstrates that the compose power sparing is at any rate 49%.Both understood postponement and static commotion edge are kept up after cautiously measuring the phone transistors.

**Keywords** —VLSI Chip, Low power, SRAM cell.