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Emerging Trends In Design Of Low Power High Speed Level Shifters In VLSI Design

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Abstract - Efficiency is one of the most important considerations in system – on a- chip designs. Various techniques were developed for reduced power consumption through reduced supply voltage. Multi supply voltages were also considered. Multiple supply voltage circuits need level conversion between different voltage domains, maintaining the overall robustness of the design. This is achieved by the application of level shifter (LS) circuits. Level shifter is an interfacing circuit which interfaces low core voltage to high core voltage and vice versa. LS facilitates communication among different modules. However literature reported that the conventional level shifters suffer from delay variation due to different current driving transistors along with huge power dissipation. The present work aims at identifying the limitations and design considerations of existing LS, through an extensive literature survey and to fix the current state of the application of LS. The survey concentrates on power consumption, power generation, multiple supply voltage, speed of processing etc in ICs. This detailed literature review is expected to pave way for addressing all the issues and challenges and helps in designing and developing highly efficient low power multi voltage high speed level shifters in the design of VLSI circuits. The major issues and challenges are listed. The results are discussed and the major conclusions drawn out of the present work are reported.