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A Performance Analysis of Pim and Tiled Processing

S. Thomas

Abstract : Literature reported that trends in microprocessors of increasing die size and clock speed and decreasing feature sizes have fueled increasing performance . However , the limited improvements in DRAM ;atecy and bandwidth and diminishing returns of increasing superscalar ILP and cache size have led to the proposal of new microprocessor architectures that implement processor - in memory , stream reccessing and tiled processing . Each architecture is typically evaluated separately and compared to baseline architecture. In this process we evaluate the performance of processors that implement these architectures on a common set of signal processing kernels . The implementation results are compared with the measured performance of a conventional system based on the power PC with AltiVec . The results show that these new processors show significant improvements over conventional systems and that each architecture has its own strength and weaknesses .