International Journal on Recent Researches In Science, Engineering & Technology
(Division of Computer Science and Engineering)
A Journal Established in early 2000 as National journal and upgraded to International journal in 2013 and is in existence for the last 10 years. It is run by Retired Professors from NIT, Trichy. It is an absolutely free (No processing charges, No publishing charges etc) Journal Indexed in JIR, DIIF and SJIF.
Research Paper
Available online at: www.jrrset.com

ISSN (Print) : 2347-6729
ISSN (Online) : 2348-3105
Volume 3, Issue 12, December 2015.
JIR IF : 2.54
DIIF IF : 1.46
SJIF IF : 1.329

A Parallel Architecture of Radix-5 DIF FFT

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Abstract- In this paper, the high performance of parallel architecture based Radix-5 DIF FFT has been presented. Cyclic distribution is used to all- to -all communication in the parallel FFT algorithms. The input and output data's are in normal order. The parallel FFT algorithm is suitable for machine-dependent because of architectural differences in the processing elements of distributed memory parallel computer. The radix-5 FFT which is used to reduce the adders and multipliers in the FFT processor. The main aim is reduces the occupied slices, LUTS and Latency.
Keywords: Radix-5, Fast Fourier Transform (FFT), Look Up Tables (LUTs).

1. Introduction

The FFT processor is a main block in those fields based on orthogonal frequency division multiplexing (OFDM) technology. The parallel FFT is a particular class of FFT algorithms which can compute the FFT in a serial manner. This algorithm needs less computation due to its recursive operator named butterfly. This operator performs the computation of complex terms, which includes multiplication of input data by appropriate coefficients.

For typical FFT/IFFT implementation, general purpose DSP processor takes approximately 1ms, which is far from the implementation using more specialized implementations. Hence, the general purpose DSP processor is not applicable for high speed and low power applications due to the lack of throughput requirement. In other hand, general purpose processors are designed to execute multiple applications and perform multiple tasks.

On-chip ROM is used available in programmable FFT processor to store the sine and cosine coefficient values. This type of programmable FFT specific processor are often provided with windowing functions in either time or frequency domain.In this paper, parallel architecture of Radix-5 DIF FFT has been proposed.

2. Literature Survey

The parallel structure of forward FFT Architecture has been explained in [1]. These structures are used for reducing the hardware of FFT and also for improving its performance. Area-efficient and energy-efficient architecture for radix-2 DIT real-valued FFT is presented in this paper. The importance of FFT in mobile communications is explained in [2].It is very important in OFDM transceiver systems. The verification and implementation is the significant role in the FFT design. [3] is presented in the parallel architecture of FFT processor for VLSI implementation.

Low-cost VLSI algorithm for discrete Fourier transform has been explained [4]. Nowadays due to the emergence of biomedical signal processing, and wide applications of real-valued time-series analysis efficient realization of FFT of real-valued signals has received further attention. Adaptive frequency transformation technique is designed with the help of Radix-2 and Radix-4 FFT architecture has been presented in [5]. From the consideration it is clear that Radix-4 structure have the half of the computational complexity of Radix-2 FFT architecture

The radix 3 and radix 5 FFT kernels of hardware implementation has been explained in [6] for LTE systems. In [6] explained the reconfigurable structure of Multiplierless Processing Element.

3. Proposed Parallel Architecture of Radix-5 DIF FFT

In this paper, the parallel architecture of radix-5 DIF FFT has been proposed. In this architecture can be factored into the multiples of 5, that is $N=5^n$. Compared to radix-2 and radix-3, radix-5 has less number of addition and subtraction.

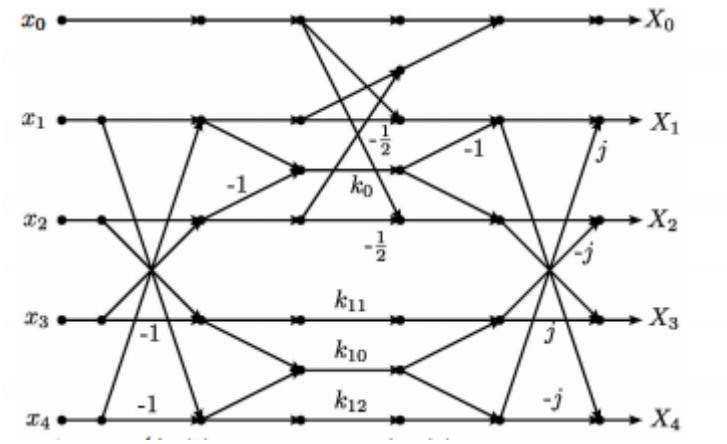


Fig.1 Parallel Architecture of Radix-5 FFT

The unit of radix-5 FFT has 4 internal multiplications, and additionally two trivial divisions by 2.Fixed radix FFT's such as radix 5 FFT are assumed to be competitively capable to radix 2 FFT. A new algorithm of parallel radix-5 DIF FFT has been designed to reduce the number of multiplications. In this radix-5 FFT, the ripple carry adder has been used to perform addition operation to reduce the power consumption and also to improve the performance of the FFT processor.

4. Results and Discussion

The proposed parallel radix-5 DIF FFT has been designed by using Modelsim 6.3C. The result of radix-5 DIF FFT is shown in Fig.2.

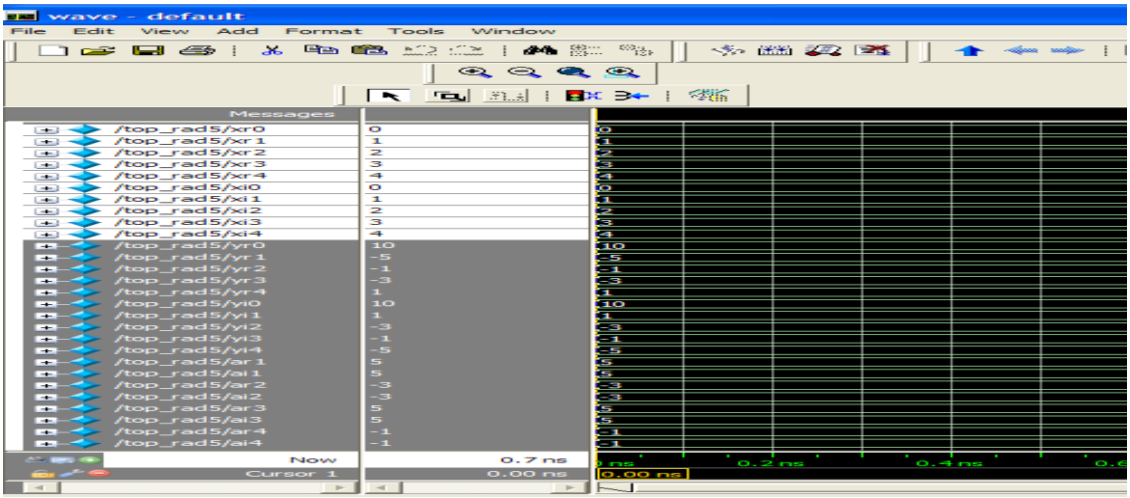
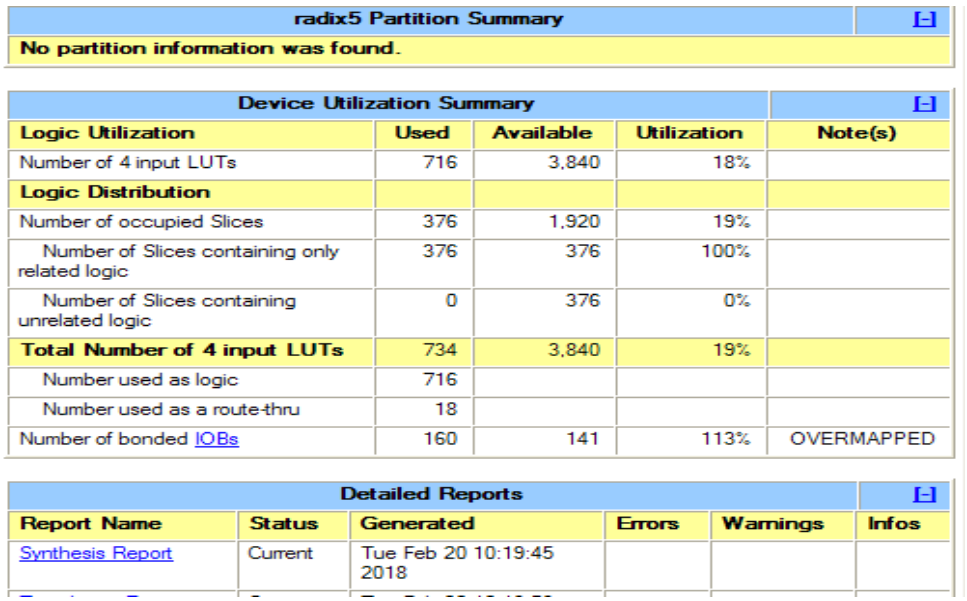


Fig.2 Simulation result of radix-5 FFT



radix5 Partition Summary
No partition information was found.

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	716	3,840	18%	
Logic Distribution				
Number of occupied Slices	376	1,920	19%	
Number of Slices containing only related logic	376	376	100%	
Number of Slices containing unrelated logic	0	376	0%	
Total Number of 4 input LUTs	734	3,840	19%	
Number used as logic	716			
Number used as a route-thru	18			
Number of bonded IOBs	160	141	113%	OVERMAPPED

Detailed Reports					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Tue Feb 20 10:19:45 2018			

Fig 3. Synthesis result of parallel radix-5 FFT for area consumption

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TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRA
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
No clock signals found in this design

Asynchronous Control Signals Information:
-----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -5

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 36.683ns

Timing Detail:
--------------
```

Fig 4. Synthesis result of parallel radix-5 FFT for delay consumption

The synthesis result of parallel radi-5 FFT and delay has been shown in Fig.3 and Fig.4. The number of occupied Slices and LUTs are 376 and 734. The delay value is 36.663 ns.The comparison analysis of existing parallel radix-2 FFT and proposed parallel radix-5 FFT is shown in Fig.5.

Methods	Slices	LUTs	Delay (ns)
Existing Parallel Radix-2 FFT	536	890	38.124
Proposed parallel radix-5 FFT	376	734	36.663

Table 1. Comparison analysis of existing parallel radix-2 FFT and proposed parallel radix-5 FFT

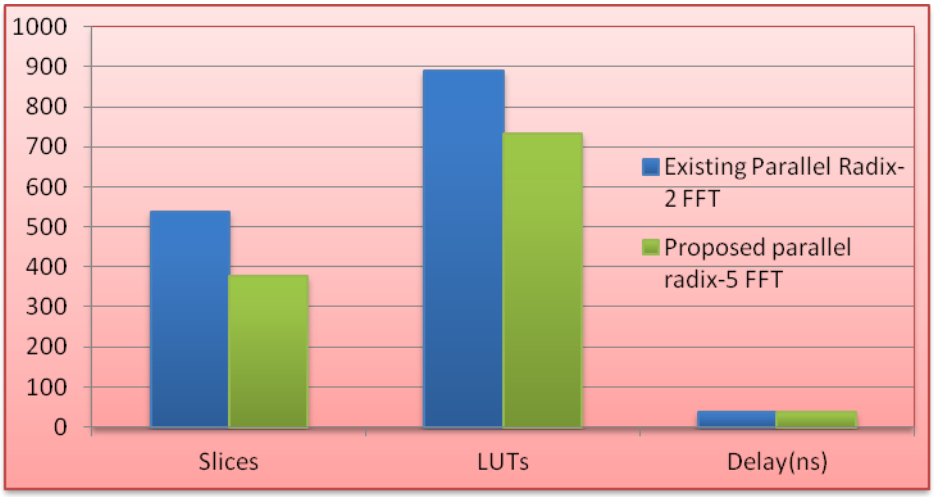

Fig.5 Performance Evaluation of existing radix-2 and proposed radix-5 FFT

5.Conclusion

In this paper, the parallel architecture of radix-5 Decimation in Frequency (DIF) FFT has been proposed. Radix-5 FFT is used for reducing the adders and multipliers. Ripple carry adder is used to addition operation in this paper. The proposed radix-5 FFT offers 29.85% reduction in slices,17.52% reduction in LUTs and 3.832 % reduction in delay elements than the existing method. Compared to radix-2 FFT, the radix-5 FFT gives better performances.

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