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An Overview of Various Domino Logics in CMOS Technology

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Abstract: Dynamic power dissipation is dominant over static power in VLSI design technology, but in contrary the static power increases due to increased leakage as technology scales down and VDD is also scaled down. The CMOS technology mainly depends on the parameters such as area, delay and power. With the purpose of reducing area, and especially increasing the switching speed by avoiding as much as possible the use and operation of slower pull-up PMOS transistors, the domino logic was introduced but it leads to more power dissipation and also results in speed-noise margin tradeoff. In this paper, various domino logics have been discoursed to reduce any of those problems.