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DESIGN AND ANALYSIS OF TESTABLE SEQUENTIAL CIRCUITS USING REVERSIBLE LOGIC

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Abstract : Testing is a process used to verify the correctness of the systems. In this project testing is carried out to detect the two stuck at fault namely stuck at 0 and stuck at 1. Here, the sequential circuits are designed based on conservative logic gates which automatically detect the two stuck at faults. Any sequential designs can be tested for classical unidirectional stuck at faults using only two test vectors such as all 1s and all 0s. Two vectors testable latches, master-slave flip-flops and dual edge triggered flip-flops are designed. The importance of this design lies in the fact that it provides the design of reversible sequential circuits completely testable for any stuck at fault by only two test vectors. There by eliminating the need of any type of scan-path access to internal memory cells. The sequential circuits are simulated using Xilinx 13.2 version. This method provides 100% fault coverage for single missing/additional cell defect in the quantum dot cellular automata (QCA) design of Fredkin gate. The layout of the Fredkin gate was simulated by using QCA designer.