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Design of Low Power and Area Efficient Multiplier for Arithmetic Logic Unit

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Abstract: In this paper, efficient multiplier is designed based on gate diffusion input technique which is the part of the arithmetic logic unit. The multiplier designed here are array multiplier and Vedic multiplier by using Gate diffusion input technique which allows reduced power consumption and optimized area for digital circuits. The existing design which is popular in low power digital circuits is pass-transistor logic. But major issues are threshold drop across the pass transistor which slows down the operation at low power supply and direct-path static power dissipation occurs. The work evaluates and compares the performance of optimized area and the reduced power of the multipliers using Gate diffusion Input and CMOS technology with the help of Tanner 14 EDA S-edit Tool. This technique is simple and also cost effective. The proposed system verifies Gate Diffusion Input technique results in decreased area and optimized power when compared to CMOS technology.