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Analysis And Design Of Vlsi Based Integer Dct Architecture

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Abstract: Discrete cosine transform is the most widely used transformation technique in image and video compression standards. The previous compression standards used floating point transforms. The conventional discrete cosine transforms (DCTs) is real-valued transforms that map integer-valued signals to floating-point coefficients. Floating-point implementations in hardware are slow so it requires too much area. In the field of VLSI, it is well known that floating-point multiplication is the operation consuming the more time so that the device becomes large and expensive. The DCT implementations based on integer approximation are currently modern transform technologies adaptable to available resources. Integer discrete cosine transform (DCT) architecture is developed based on the Multiple Constant Multiplication (MCM)-based hardware oriented algorithm with only binary additions and shifts to be used in HEVC. The one dimensional eight point DCT is designed by using two different architectures such as generalized and reusable. These two architectures have been coded using verilog HDL (Hardware Description Language). These architectures were simulated and verified using Cadence 180 nm NC LAUNCH tool and also synthesized using Cadence encounter and the area, power for the architecture is determined.