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Automating the Digital Circuits for SoC Low Power Designs considering various Power Management Techniques using Cadence Encounter

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Abstract: This paper, handles the detailed design flow for automating digital circuits by accounting the prominent effects and sequences of various powers and the different techniques to minimize its adverse effects. The power management techniques like Multiple Supply Voltage (MSV) technique which is adopted to operate different functional blocks at different supply voltages as per the performance requirement of the chip, the Power Shut-Off (PSO) technique which switches off the power to parts of chip when the blocks are not used, and Dynamic Voltage and Frequency Scaling (DVFS) technique where the selected portions of the device are dynamically set to run at different voltages and the frequencies on the fly while the chip is running. Low Power Synthesis is done for any SoC design using the Cadence RTL compiler where the low power design is synthesized to gate level netlist. The synthesized netlist is used for the physical design implementation which is then subjected to complete physical design verifications. Almost 60% of leakage power, 58% of dynamic power, and 94% of total power are reduced subjected to these power management techniques.