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High Performance Floating Point Unit

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Abstract: The benefits of floating-point arithmetic over fixed-point arithmetic comes from its constant relative precision over a wide dynamic range. However, floating-point operations require complex processes such as alignment, normalization and rounding, which increases the area, power consumption and latency. In order to reduce the overhead, fused floating-point units such as Fused Multiply-Add (FMA), fused add-subtract (FAS), fused dot product (FDP) have been proposed, which execute several operations in a single unit to reduce the area, power consumption and latency. The fused floating point adder has been implemented in 8 point DIF FFT butterfly operation. The fused floating-point adder/subtractor performs two operations in a single unit to achieve better performance and better accuracy compared to a network of discrete floating-point adders. The simulation results are obtained by using simulation Softwares.