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Static and Dynamic Noise Margin Analysis of Sub-threshold Average-8T SRAM Architecture

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Abstract: Technology scaling in sub-threshold regime has significantly shrunk the SRAM stability in data retention, read and write mode of operation. This work presents a new Average-8T SRAM architecture providing good noise margins during read and write mode. This paper also describes the power analysis of the SRAM cell when operating the cell in sub-threshold regime. Furthermore, the weak on currents which are crucial in sub-threshold regime are well carried out by the application of low leakage techniques in this paper. Importantly, this paper improves the robustness of an SRAM cell and implements the cell in power constraint applications. The stability of the proposed Average-8T SRAM cell has been calculated from N-Curve where it measures various metrics related with stability. The delay parameter is measured for Average-8T SRAM cell and uses a Dual-edge transmission gate in the design to improve the speed and to achieve a successful write.