International Journal on Recent Researches In Science, Engineering & Technology
(Division of Electronics and Communication Engineering)
A Journal Established in early 2000 as National journal and upgraded to International journal in 2013 and is in existence for the last 10 years. It is run by Retired Professors from NIT, Trichy.
It is an absolutely free (No processing charges, No publishing charges etc) Journal Indexed in JIR, DIIF and SJIF.
Research Paper
Available online at: www.jrrset.com
Chief Editor : Dr. M.Narayana Rao, Ph.D., Rtd. Professor, NIT, Trichy.

ISSN (Print) : 2347-6729
ISSN (Online) : 2348-3105

Volume 3, Issue 4, April 2015

JIR IF : 2.54
DIIF IF :1.46
SJIF IF: 1.329

A 6-bit High Speed Subranging ADC in 45nm CMOS

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Abstract: A 6-bit, subranging analog to digital converter (ADC) implemented in 45-nm CMOS is developed. CMOS technology holds out the promise of a mixed signal circuit integrated on a single chip along with logic and memory circuits to form a system-on-chip. Scaling down of CMOS technology reduces the supply voltage and the effective signal swing range, while noise keeps the same. This poses great challenges on the design of high speed low power and more accurate ADCs. The typical flash ADC requires (2^n–1) comparators for converting an analog signal into 'n' bit digital signal with a very high digitizing rate. Subranging ADC on the other hand uses fewer comparators, draws less power, has lower input capacitance, and can attain higher resolutions at the expense of speed. In this project, a CMOS low power subranging Analog-to-Digital Converter (ADC) is designed with improved performance compared with the conventional subranging ADC. The ADC has the three main blocks, the coarse decision Flash ADC, fine decision Flash ADC and control clock. The control clock is the main block which is used to control the blocks such as sample and hold, the coarse and the fine decision flash ADCs. Here the analog input is first passed into the sample and hold circuit, the analog signal is sampled at the positive edge and is hold till the end of the conversion. The sampled analog signal is passed into the coarse flash ADC to get the higher order bits, and converted back into analog signal using DAC. The difference between the analog signal and the converted analog signal is given to the fine ADC to get the higher order bits for achieving the same resolution as that of flash ADC with less number of comparator to achieve low power as compared to the flash ADC.