Optimization of Multi Precision Multiplier using Parallel Prefix Adder

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Abstract: A multiplier is one of the key hardware blocks in most digital and high performance systems such as DSP and microprocessors etc. With the advancement in the technology, many researchers have tried and are trying to design multipliers which offers either high speed or low power consumption. In this project, the speed of the multiplier is compared by replacing different types of adders in the proposed Multi Precision Multiplier. Since speed is one of the most important criteria, any one of the adders Viz. Kogge Stone adder, Carry look ahead adder, Han-Carlson adder, superset adder, Brent kung adder is preferred. In this project, initially the architecture of a multi precision multiplier is designed and then use the above mentioned few adders in it for the fastest multiplier operation.