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A Survey Of Various Leakage Reduction Techniques In Semiconductor Memories

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Abstract: Low power design circuits have a major influence in achieving a longer lifetime of the battery in almost every portable device. In deep submicron process[1], to improve the performance and functionality of a chip, scaling must be done. Due to scaling of the feature sizes the device's speed, operating frequency and performance has been improved [3]. But the power consumption will be higher. In order to reduce the power consumption of a device, the supply voltage is scaled and to make the highperformance, thethreshold voltageof the device is also needed to be scaled down. As the Vth is reduced by scaling, the sub-threshold current increases rapidly and it causes the leakage power to a greater extent. Thus leakage power becomes a major contributor for total power dissipation of a circuit.The establishment of static power consumption in CMOS strategies becomes one of the aggressive effects of scaling technology. Physically, when the feature sizes neglected the nanometer disorder, the CMOS transistor acts as an effective perfect ideal switch, only whenthe transition occurs. However, static power influences all kinds of CMOS circuit, it is precisely critical for SRAMs. Here the number of transistors is high, so it leads to high reduction of leakage [6]. As per the aggregate technology, the SRAMcell usage has been enlarged to superior level, though enterprising the system on-chips in CMOS expertise.