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Performance Evaluation of Different Multipliers in VLSI

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ABSTRACT: High speed and low power multiplier is utmost requirement of today's VLSI systems and digital signal processing applications like FFT, Finite impulse response filters, convolution etc. In this paper, we have discussed different types of multipliers like booth multiplier, Wallace tree multiplier, array multiplier and double throughput multiplier. Each multiplier has its own advantages and disadvantages. Different types of techniques are presented for improving the speed and low power consumption like pipelined booth multiplication technique in which pipelining is used in booth multiplier to reduce the delay of each stage. Apart from conventional multipliers, double throughput multipliers can be used to get double output in single multipliers.

KEYWORDS: DSP, Array Multiplier, Array Multiplier, Booth Multiplier.

I. INTRODUCTION

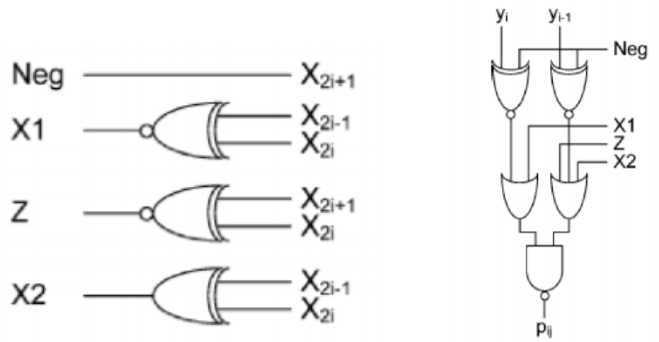
Multipliers have massive space, long latency and consume considerable power. Reduction of power consumption makes a device reliable. Therefore low power multipliers with high clock frequencies play a crucial role in today's digital signal processing. Digital signal processing (DSP) is that the technology at the center of succeeding generation of private mobile communication multiplication systems. Most DSP systems incorporate a multiplication unit to implement algorithms like convolution and filtering. Low power consumption and smaller area are some of the most important criteria for the fabrication of DSP systems and high performance systems. With advances in technology, many researchers have tried and are trying to design multipliers which offer either of the following design targets – high speed, low power consumption, regularity of layout and hence less area or even combination of them in one multiplier thus making them suitable for various high speed, low power and compact VLSI implementation[1-3]. Paper is organized as follows. Section II describes modified booth multiplier, section III and IV deals with Wallace and double throughput multipliers. In section V comparison of discussed multipliers were made on FPGA platform.

II MODIFIED BOOTH MULTIPLIER

It is a powerful algorithm for signed-number multiplication, which treats both positive and negative numbers uniformly [1-3].For the standard add-shift operation, each multiplier bit generates one multiple of the multiplicand to be added to the partial product. If the multiplier is very large, then a large number of multiplicands have to be added. In this case the delay of multiplier is determined

mainly by the number of additions to be performed. If there is a way to reduce the number of the additions, the performance will get better.

Modified Booth multiplier it has only three major steps compared to normal booth multiplier. The first step is generating the partial product through recoding, the next step is reduction of partial products and the last step is adding of partial products to produce final result. For deeply knowing modified booth algorithm we need to understand each stages. Modified Booth uses encoder and decoder for generating partial products. The computation time of Modified Booth multiplier is proportional to logarithm of the word length of operands. So using this multiplier we can reduce half the partial products. The modified booth encoder does the job of recoding and generating certain signals called negate,single, double and zero. The recoding is done by grouping the multiplier X. During grouping overlapping occurs. Its starts from the least significant bit where also a zero is addedas LSB and is grouped[4].



(a) (b)

Fig 1. MODIFIED BOOTH (A) ENCODING AND (B) DECODING

III. WALLACE TREE MULTIPLIER

Wallace Tree Multiplier The speed of multiplier is depends on the total time taken for summation of partial products. Wallace tree multiplier is faster than Array multiplier. Scientist Chris Wallace in 1964 introduced an easy and simple way of summing the partial product bits in the parallel using the tree of the Carry Save Adders which is known as “Wallace Tree” [2]. Wallace tree multiplier uses carry save addition algorithm. A typical Wallace tree architecture is shown in figure 2.

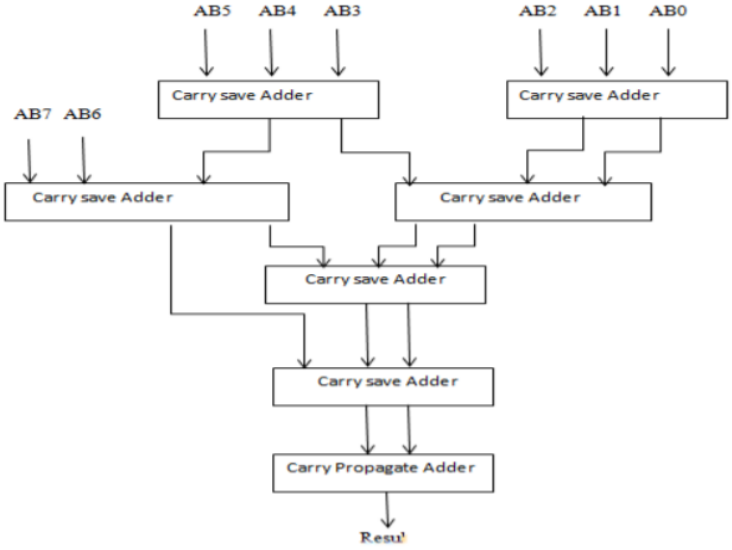


Fig.2 Wallace Tree Multiplier

Wallace multiplier includes some steps to multiply two numbers .The first step is formation of the bit products. Then carry save adder reduces bit product matrix into two row matrix. After that the remaining two rows are summed by using the fast carry propagate adder to produce the final result [6].

IV. Double throughput multipliers

In [7], double throughput is realised effectively by adopting Twin precision (TP) technique in MB multiplier. MB algorithm [8] is a widely used signed algorithm since it has reduced partial product row. The possibility of combining N and N/2 bit (b) multiplication in the same N b tree multiplier is called as TP multiplier where N is the bit width of the multiplier. Here we can split the partial product bits of the N b multiplier in such a way that N/2 b multiplication can be performed in the least significant part (LSP) of the multiplier in parallel with another N/2 b multiplication in the most significant part (MSP). And this is done in the partial product reduction tree without inclusion of any additional logic as explained in [9]. Multiplexers (muxes) are generally employed in TP multiplier to select appropriate partial product for N and N/2 b multiplication.

V. COMPARISON

Based on three parameters TIME/DELAY, POWER and AREA a comparison were made for modified booth, array, Wallace and double throughput multipliers. The power is calculated for 250 Hz clock cycle using Spartan 3E Power Estimator. The table 1 shows the comparison 0f different multipliers in FPGA environment.

PARAMETERS	MODIFIED BOOTH	ARRAY	WALLACE	DOUBLE THROUGHPUT
DELAY(ns)	20.16	62.74	52.33	35.75
POWER(mw)	87	183	160	125
AREA (LUTs)	8%	45%	40%	22%

Table 1 comparison of different multipliers

V. CONCLUSION & FUTURE SCOPE

In this paper, multipliers for low power applications were implemented. Modified booth, array, walllace and double throughput multipliers were implemented on Spartan 3E XLINX 13.1 version. The Power, Delay and Area are calculated for these multipliers. Power measurements were performed using Xilinx power estimator. From the table1, it is evident that Modified Booth multiplier requires less time, low power and less area to implement compared with other multipliers.

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