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Design of High Gain Low Voltage CMOS Operational Amplifier

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Abstract
This paper provides a design of High attain two stage CMOS operational amplifier, which operates at ±2.5V strength grant the use of tsmc 1um CMOS technology. The OPAMP designed has two-stages and a single ended output and is designed to show off a attain bandwidth of 12MHz, acquire of 81.52dB with a 62 degree phase margin and 45 degree acquire margin to work with a load capacitance of 10pF and have energy dissipation 0.7mW. The Operational Amplifier is deliberated using RC Compensation for stability. Design and Simulation erstwhile carried out in P Spice.
Keywords - RC Compensation, Slew Rate , CMOS Op-Amp, Gain, Stability

I. Introduction

The Operational Amplifier (Op-Amp) is a very primary building block in Mixed Signal design. Basically, Op-Amps are voltage amplifiers being used to get high obtain by way of making use of differential inputs. The acquire is usually between 50 to 60 decibels. Two levels Op-Amp is one of the most normally used Op-Amp architectures. The constantly scaling of transistor size allows the more quantity of transistors on the same dimension of chip which reducing time delays [2]. This effects in non-stop increase in the processing capacity and operating frequency. Operational Amplifiers is used very oftentimes in digital circuits. Op-Amp based circuits are extra precise, noise insensitive and are less influenced to fluctuations. The large task is to Design a steady operational amplifier with a excessive gain and high reap bandwidth with reducing voltage furnish and channel length. Trade off amongst various parameters such as power dissipation, bandwidth, speed, attain has to face while designing Op-Amp [1]. With higher achieve and bandwidth the pace and accuracy of the amplifier increases however the balance in poor remarks decreases. One of the primary boundaries of op amp is that they are no longer particularly fast. The traditional performance decreased hastily for frequencies which are increased than about 1 MHz, even though some models the use of different method are designed especially to handle higher frequencies [4]. To diagram a stable Op-amp with higher frequency always a large task. Aim is to construct an Op-Amp with a pretty giant obtain and comparatively excessive cohesion achieve bandwidth at a maximum segment margin and obtain margin to make sure stability. Various compensation methods can be adopted to attain this. In this paper a two stage CMOS Op amp is designed with high acquire and stability.

II. CMOS OP AMP Architecture

The decreased channel size gadgets places new challenges in designing of Op-Amps places in low energy applications with reduced channel size devices. Advancements which have appeared lately through new methods and technologies, provide us extra choices in implementations. Two stage CMOS Op–Amps has two dominant poles the section margin ought to e reach to less than the quantity without difficulty which is simply ample for stable operation. The hassle like this must be seem by using designers, in any other case there will be possibility that the output of Op-Amp will oscillate and

it will come to be an oscillator as a substitute of an amplifier. In some purposes the reap and/or the output swings provided by way of cascade op-amps are now not adequate. For these cases, we used "two stage" Op-Amps, with the first stage providing a excessive reap and the second, large swing. In amplifier employing the negative comments frequency compensation approach is used to enhance stability.

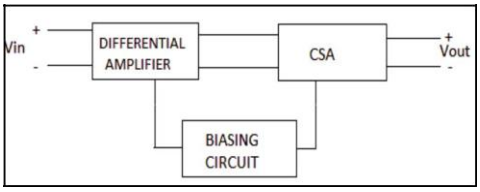


Fig. 1: Two Stage Operational Amplifier

Two stage operational amplifiers consist of a differential amplifier in the 1st stage accompanied by means of a Common Source Amplifier in the 2nd stage. Differential Amplifier stage is to make certain high acquire and CSA stage is to similarly amplify the attain an also supply high voltage swing at the output. The block graph of a two stage CMOS Operational amplifier is shown in fig. 1. The 1st block is a differential amplifier. It has two inputs, non inverting input and inverting input. It can provide a differential voltage or single ended voltage, decided with the aid of configuration at the output which depends on differential input voltage. Single ended output reduces the output swing of the amplifier. The Common Mode Rejection Ratio is additionally degrades as the symmetry of the circuit is lost.

The differential amplifier stage is not ample in some circuit, extra amplification required is provided through the 2d stage, which is the frequent source amplifier, and it is pushed by means of the output of the differential amplifier stage. The biasing circuit included to supply the acceptable running factor to each transistor in its saturation place [2]. At the stop to provide the low output impedance, an output buffer stage can be connected and large output present day needed to drive the load. Output buffer is now not required for a small capacitive load. When the output buffer stage is no longer used, the circuit turns into an operational transconductance amplifier or OTA.

III. Op-Amp Architecture

The circuit consists of three subparts: the differential obtain stage, 2nd obtain stage and biasing circuit. MOSFETS M1, M2, M3, M4, M5 form the primary stage which is differential amplifier phase. M6 and M7 shape the 2d reap stage and are in Common Source Amplifier Configuration. M8 and the Current supply shape the biasing circuitry. M9 and the Compensation capacitor provide frequency compensation wanted for stability. To make Op amp stable proper hand pole is major concern. To put off the right hand pole we use rc compensation technique.

A. Differential Gain Stage

The differential achieve stage consists of MOSFETS M1, M2, M3, M4 and M5 as proven in fig. 2. Positive input signal is applied to the gate of M1 and poor enter is given to the gate of M2. An lively load which is a present day mirror made up of M3 and M4 is used in this stage. The obtain of first stage is the transconductance of M1 multiply with the aid of the total output resistance considered at the drain of M2. The output resistance is primarily contributed through the enter transistors themselves and additionally the output resistance of the load transistors, M4 and M3. The lively load cutting-edge mirror used in this circuit has three primary advantages. First, the chip area occupied is small and gives comparatively massive output resistance. The present day reflect presents the differential enter to single - ended output, and finally, the load helps with common mode rejection ratio. In this, the differential enter to single ended output is performed with the aid of using a contemporary replicate (M4 and M3). The current is mirrored by means of M3 and M4 from M1 and subtracted from the present day from M2. Finally, the output resistance of the enter stage is expanded by differential contemporary from M1 and M2 gives the single-ended output voltage, which is the section of the input to the next stage. The transconductance of this stage is clearly the transconductance of M1 and M2.

$$g_{mI} = g_{m1} = g_{m2}$$

B. Common Source Amplifier Stage

The 2nd stage consists of a frequent supply amplifier which acts as a present day sink load inverter. The purpose of the 2d gain stage is to provide additional attain and it consisting of transistors M6 and M7. The output of first stage is the center to this stage. It consists of a capacitor to travel the pole which is lowly in frequency to higher frequency. Due to this movement of pole the steadiness of the amplifier is increased. For balance CCgt;0.22CL.

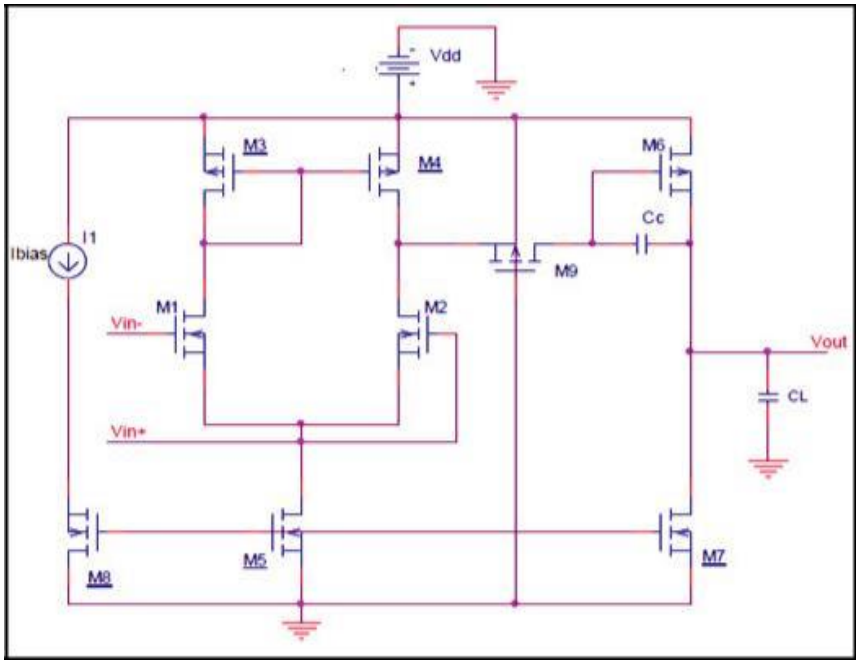


Fig. 2: Two Stage Op-Amp Circuit

M6 the general source amplifier amplifies the output comes from the drain of M2. M7 is lively load transistor, which serve as the load resistance for M6 in this stage. This stage has obtain which is the equivalent load resistance considered at the output of M6 and M7 elevated with the aid of the transconductance of M6. M6 is the driver while M7 acts as load. The transconductance of this phase is the transconductance of M6.

$$g_{mII} = g_{m6}$$

C. Biasing Circuit

Current source, I1 in figure. 2 acts as a indication source for transistor M8. I1 and M8 structure a current reflect biasing network using the transistors, M5 and M7 which act as present day sinks. The bias network controls the gate to source voltage of M5 and M7. Biasing is wanted to make all transistors to work in saturation region. If we make bigger the size of M5, slew rate and segment margin will be increase.

D. RC Compensation

R and Cc are used between gate and drain of M6 to improve the section margin and as a result stability of the circuit. For this purpose rather of resistance a MOS transistor is used.

IV. Design of the Two Stage Op AMP

The first factor viewed in the sketch was once to meet the favored specifications. Based on a clear understanding of the specifications, the standard CMOS Op-Amp circuit topology in this graph has been chosen.

Table 1: Specification of two-stage CMOS op-amp

Specification Names	Values
Supply Voltage	± 2.5V
Gain	> 80db
Gain Bandwidth	≥ 10Mhz
Slew Rate	20V/μSec
Output Swing	± 2.5V
Common Mode Rejection Ratio	> 60db
Phase Margin	≥ 60˚
Power Dissipation	≤ 1mW
ICMR	-2.5V To +2.5V

A. Design Methodology

The DC gain of the first stage is

$$A_1 = -\frac{g_{m2}}{g_{ds2} + g_{ds4}}$$

The DC gain of the second stage is

$$A_2 = -\frac{g_{m6}}{g_{ds6} + g_{ds7}}$$

Overall gain of the Op-amp is

$$A_V = A_1 . A_2$$

$$A_V = \frac{g_{m1} g_{m6}}{(g_{ds2} + g_{ds4})(g_{ds6} + g_{ds7})}$$

Slew Rate of the Op-amp is

$$SR = \frac{I_5}{C_c}$$

Where I5 is the current to the M5 transistor and it is the bias current of the input stage.
The Gain bandwidth of the Op-Amp is

$$GB = \frac{g_{m1}}{C_c}$$

V. Simulation Result

A. DC Sweep

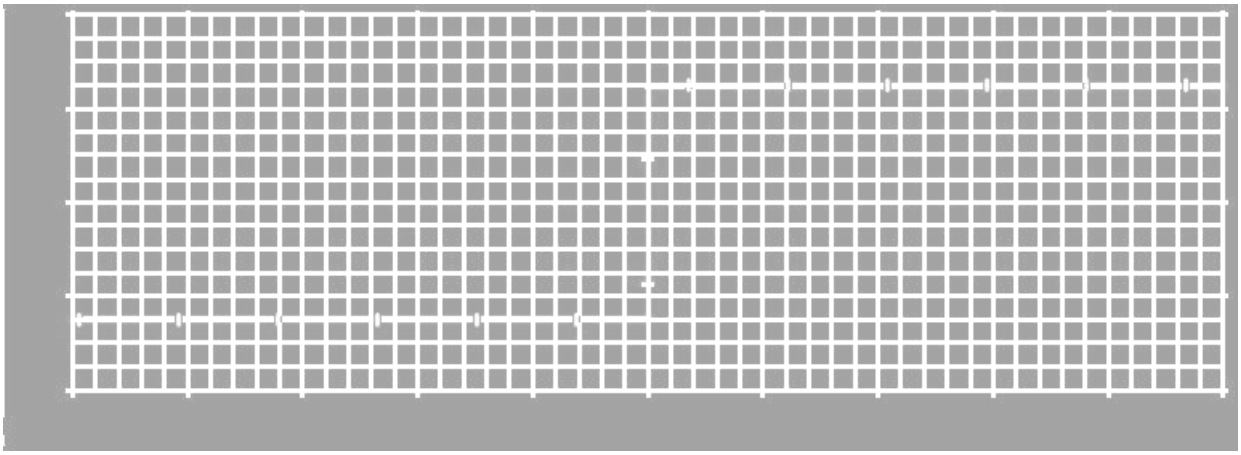
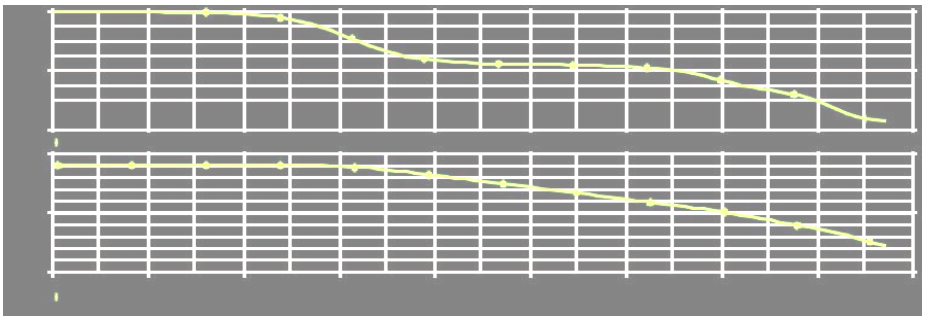
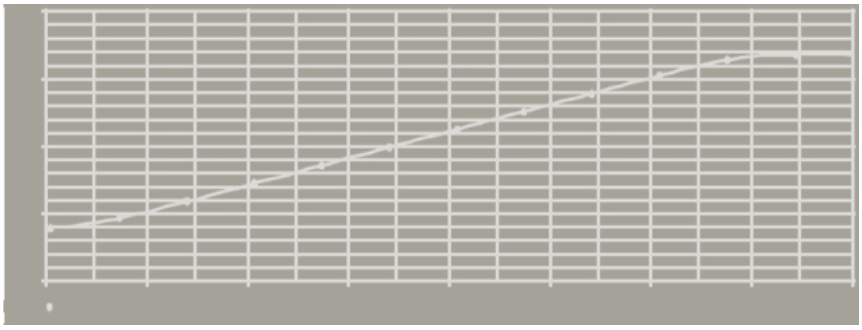


Fig. 3: Open Loop Transfer Characteristics

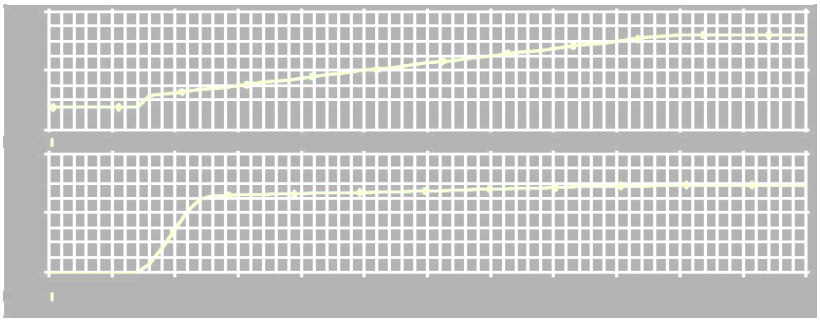
B. Frequency Response



C. Common Mode Gain



D. ICMR



E. Transient Responses

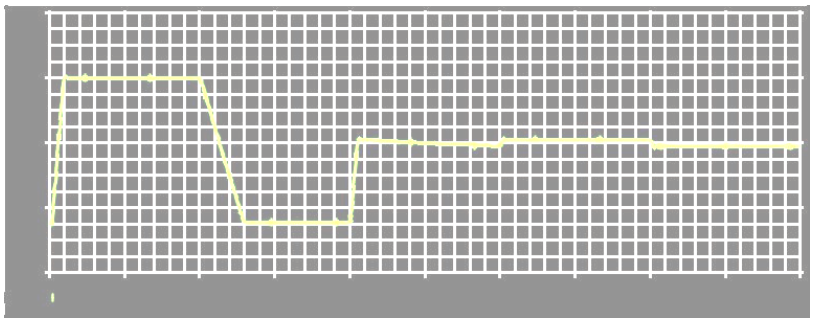


Table 2: The Geometric Dimension included and the Electrical Parameter Yielded

The Design Parameters		The Electrical Parameters Yielded	
M1	3/1 um/um	Phase margin	62˚
M2	3/1 um/um	Gain	81.51db
M3	15/1 um/um	C_C	1Pf
M4	15/1 um/um	UGB	12MHz
M5	4.5/1 um/um	ICMR	-1.2 - 2.5V
M6	94/1um/m	Slew Rate	27.87V/us
M7	14/1 um/um	Common Mode Gain	-150db
M8	5.1/1 um/um	Output Swing	± 2.5V
M9	1/1 um/um	Gain Margin	45˚
^{I}BIAS	30uA	Power Dissipation	0.7mW
^{V}DD	2.5V	Output Resistance	138.6kΩ
C_L	10PF	3db frequency	1KHz

VI. Conclusion

This paper presented the full plan and analysis of a two stage CMOS Op-Amp. The amplifier introduced in this paper operates in saturation mode and regulates its bias current. When a sign is utilized the contemporary in the amplifier will increase so that these amplifiers have very high driving current. The Op-Amp has low strength as well as low voltage. RC compensation is used for steadiness which makes Op-Amp quite stable. But there is continually some scope of improvement, right here we can enlarge reap bandwidth more with open loop gain.

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