ISSN (Print) : 2347-6729
ISSN (Online) : 2348-3105

International Journal on Recent Researches In Science, Engineering & Technology

Volume 5, Issue 4, AApril 2017.

A Journal Established in early 2000 as National journal and upgraded to International journal in 2013 and is in existence for the last 10 years. It is run by Retired Professors from NIT, Trichy. It is an absolutely free (No processing charges, No publishing charges etc) Journal Indexed in JIR, DIIF and SJIF.

JIR IF : 2.54
DIIF IF : 1.46
SJIF IF : 1.329

Research Paper
Available online at: www.jrrset.com

Functioning of Power Resourceful Vedic Multiplier using Ancient Tolerant Architecture

G.Nagarajan, V. Vijayakumar
Department of Electronics and Communications Engineering
Dhanalakshmi Srinivasan Engineering College, Tamil Nadu, India

Abstract: In this paper, we endorse a new paradigm that is a strength environment friendly and low location Vedic multiplier to meet the demand of high precision and low power integrating with the Algorithmic Noise Tolerant (ANT) architecture. The truncation mistakes can be diminished by implementing historic Vedic multiplication strategies mixed with current probability and data method. The hardware complexity of multiplier is extensively simplified. In this 12*12 bit Vedic multiplier, the wonderful whole on-chip strength can be decreased with the aid of 15% and the circuit place in our proposed format is decreased by 25% in contrast with present constant width RPR multiplier. Hence the electricity is successfully used and implemented.
Keywords: Vedic multiplier, ANT architecture, Truncation errors

INTRODUCTION

The want for ultra-low energy consumption meets the demand of the usage of portable digital devices and Digital Signal Processors (DSP). Researchers proven many low-power methods to limit the power dissipation. Supply voltage scaling is the great method to adopt in deep sub-micrometer technologies along with CMOS technologies. In prevalent power consumption of an digital circuit is proportional to the rectangular of the grant voltage (The International Technology Roadmap for Semiconductors, 2009). But the approach of Voltage Over Scaling (VOS) (Hedge and Shanbhag, 1999) leads to degeneration of noise (S/N). The complex good judgment sequential operations are carried out in DSPs like addition, multiplication etc. One of the most complex operations is array multiplication. Since the size of the array increases, the demand for energy consumption additionally will increase drastically. So in order to compensate these factors, A novel approach of Algorithmic Noise Tolerant (ANT) technique (Shim et al., 2004) adjoined with voltage over scaling in the fundamental block with Reduced Precision Replica (RPR) Research Paper to decrease the errors and also achieves the quantity of strength saving. ANT architecture has desired due to the fact it has the main advantage of lowering the truncation of soft mistakes without compromising the location of the circuit, electricity consumption and grant voltage scaling. Instead of the use of full-width rpr (Kidambi et al., 1996), the fixed width rpr is designed in the previous technique with the use of probability, statistics, and partial product time period evaluation to locate accurate compensation vector for efficient RPR design. It gives exact and environment friendly outcomes however still the problem of an location overhead. So we put in force a 12*12 ANT architecture is designed and carried out with an historical but modified Vedic multiplier (Premananda et al., 2013). So the circuit can be made less complicated and the critical course lengthen improved besides compromising the chip region and electricity consumption.
In general, the velocity of the multipliers is constrained with the aid of the pace of the adders used for partial product terms weight. The partial product terms are realized by means of the usage of carry

pass by technique. Different algorithms are used in Vedic arithmetic for multiplication. One of the first-rate and basic techniques is Urdhva Tiryagbhyam (Premananda et al., 2013). It is also regarded as a Vertical-Cross algorithm. This technique is used in quite a number branches of engineering for computation and sign processing (digital) techniques. The Vedic multiplier is built-in with the ANT architecture and calculated the error precision and the amount of power is noticeably reduced.

EXISTED ANT ARCHITECTURE DESIGN

The existed ANT structure consists of Main Digital Signal Processor (MDSP) block and Error Correction (EC) block. VOS (voltage over scaling) technique is used in MDSP block. The circuit is shown in fig 1 below. If Tcp is greater than Team of the circuit then gentle blunders will have occurred. Where Tcp is crucial path delay and Tsam is sampling period. An specific copy of MDSP but with reduced precision parameters and shorter computation prolong is used as EC. The output of MDSP is ya[n] in which there exists an quantity of input independent smooth errors. The output of RPR block is yr[n]. If Tcp is smaller than Tsam, yr[n] is applied to realize blunders in ya[n]. To obtain the errors against the threshold the difference |ya[n] -yr[n] | is considered. If the difference is large than Th then y^[n] = yr[n]. Otherwise y^[n] = ya[n]. This determined by, Th = maxvinput |yo[n] – yr[n] ...(1)
where yo[n] is error free output signal. In this technique, electricity consumption is diminished but nevertheless continues SNR degradation. Fixed-width multiplier has the gain of keep away from the usage of growing bit width in DSP applications compared to full-width multiplier design. To construct a fixed width DSP with n-bit input and n-bit output by truncating n-bit LSB output is high-quality solution. It consequences in rounding error. The rounding error can be compensated with the steady correction price (Lim, 1992; Schulte and Swartzlander, 1993; and Jou and Wang, 2000) alternatively than variable correction fee (Curticapean and Niittylahti, 2001; Strollo et al., 2005; Kuang and Wang, 2006; Petra et al., 2010; and Wey and Wang, 2010). In fixed width, the compensation error is corrected by standard truncation error of MDSP block. Error compensation algorithm makes use of partial product terms with the biggest

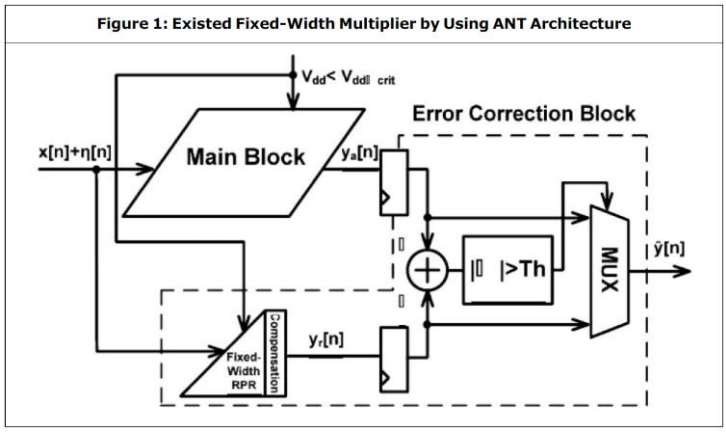

Figure 1: Existed Fixed-Width Multiplier by Using ANT Architecture

the weight of LSB with the idea of probability, statistics, and linear regression evaluation to observe error compensation cost (Jou et al., 1999). In this technique, there is no unique fixed width RPR block is designed. Fixed width multiplier circuits are built-in with a full-width multiplier circuit to compensate the error value. The Error compensation circuit ought to be located in the non-critical route of fixed-width RPR in order now not to expand the integral course delay.

Error Compensation Vector

The most important function of RPR block is to assemble the blunders took place in the output of MDSP and continues the SNR of the complete gadget while attaining the low supply voltage. The

circuit of the compensation vector is shown in Figure 2. In MDSP of ANT Baugh-Wooley multiplier of n-bit inputs of X and Y is given by using

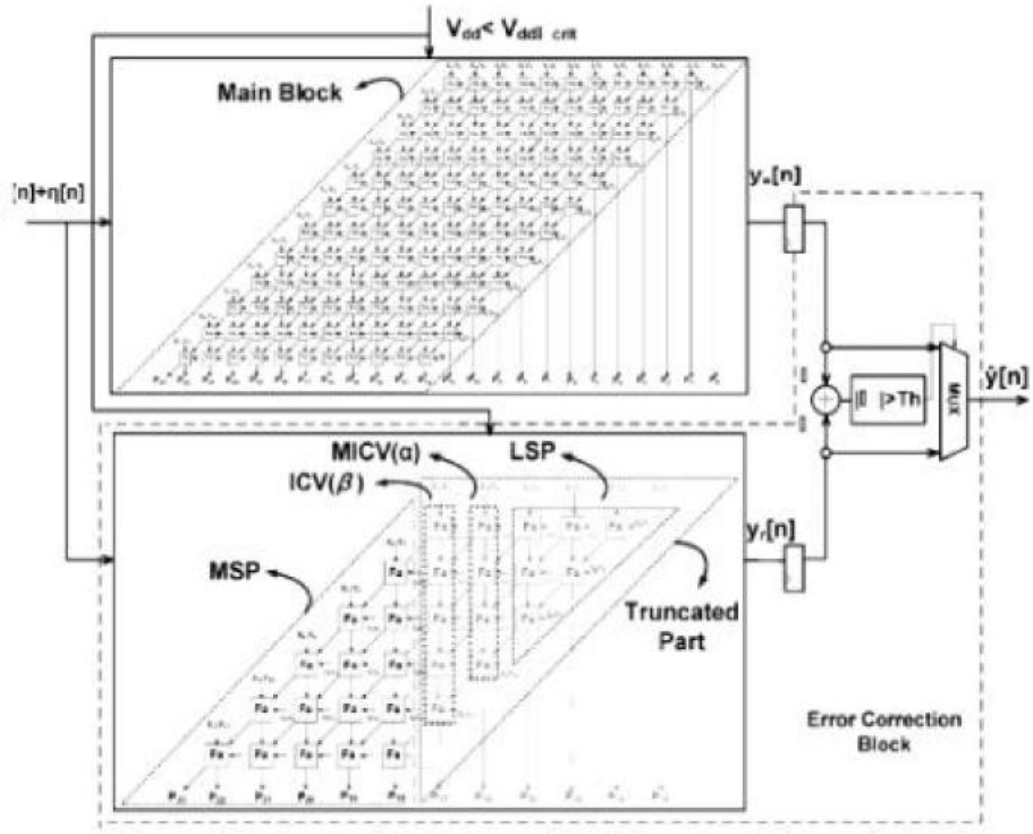

Figure 2: 12*12 ANT Multiplier with 6-Bit Fixed-Width RPR Block

$$X=\sum_{(i=o\ to\ n-1)} x_i.2^i \qquad Y=\sum_{(i=0\ to\ n-1)} y_i.2^i \qquad ...(2)$$

The multiplication result is denoted by 'P' which is

$$P=\sum_{(k=0\ to\ 2n-1)} p_k.2^k = \sum_{(j=0\ to\ n-1)} \sum_{(i=0\ to\ n-1)} x_i y_j.\ 2^{i+j} \qquad ...(3)$$

are functional to build the error compensation algorithm because they have the highest Weight.α) and MICV (β) and slightest Significant Part (LSP). Here, for the computational reason, only MSP part is there outstanding sub-sets are truncated. ICV (α), Minor Input Correction Vector MICV (βThe (n/2) bit unsigned full-width Baugh- Wooley product array is divided into 4 subsets. They are the majority Significant Part (MSP) Input Correction Vector ICV . The accuracy of fixed-width is given by

$$\varepsilon = P - P_t \quad ...(4)$$

β Is equivalent to half of α+ 1. If we examine the multiple compensation vectors for average purpose which are larger than 0.5*2(3n/2). So that we can lower the recompense error effectively. Multiple recompense vectors are constructed by combining f (ICV) and f (MICV) (I-Chyn Wey et al., 2015). The weighted vectors β and βwhere P is output of MDSP and Pt is fixedwidth RPR output. Standard truncated error is distributed between .βis equal to half of α+ 1. If we examine the multiple compensation vectors for average reason which are larger than 0.5*2(3n/2). So that we can lesser the recompense error effectively. Multiple recompense vectors are constructed by mergING f (ICV) and f (MICV) (I-Chyn Wey et al., 2015). The weighted vectors β and β.

Fixed Width RPR Multiplier with Compensation Constructed by ICV and MICV

In order to understand the fixed width RPR, we build one directly injecting ICV (…lβ = 0 and β, C (n/2)-1 which is shown in Fig. 3. Other compensation vector is build by one restricted controlled OR gate. Input of OR gate is X(n/2)Y(n-1). Other input is restricted controlled by referee whether ≠ 0 as well. Cm1 indicates the controlled input of AND gate. Cm and X (n/2) Y (n-1) are injected into 2 input OR gate. While it gives the most favorable solution in which outperform the low power consumption and area efficient architecture.

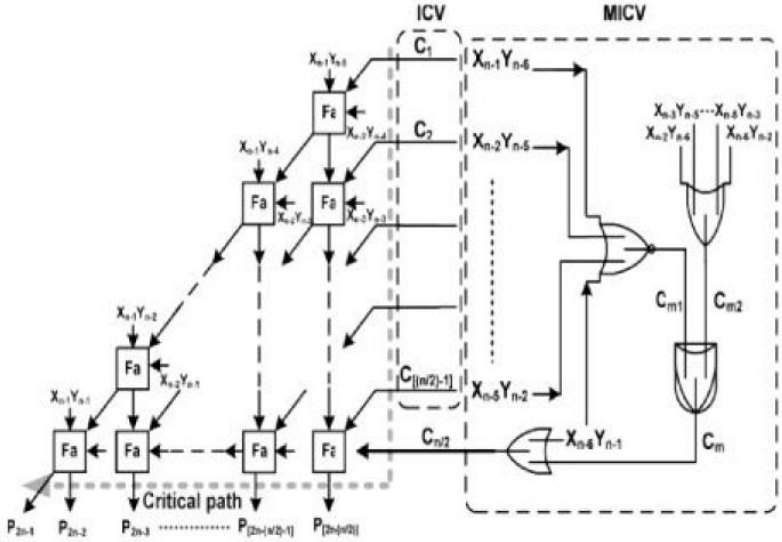

Figure 3: High Accuracy Fixed Width RPR Multiplier Combining ICV and MICV as Compensation Vectors

OVERVIEW OF VEDIC MULTIPLIER

Multipliers (Binary Multiplier) are the vital components in DSP devices. The performance of DSP processor is based on by and large complicated calculations of multipliers (Array multiplications). So the format of a multiplier in a DSP processor has a principal impact on the performance. Vedic multipliers are designed primarily based on the sixteen sutras(principles). It helps in the field of special branches of engineering for computation process. Integrating Multiplication with Vedic mathematician methods helps the saving of computation time. It enhances the pace of operation. These techniques can be at once applied to each differential and fundamental calculus of any kind.

RESUTS

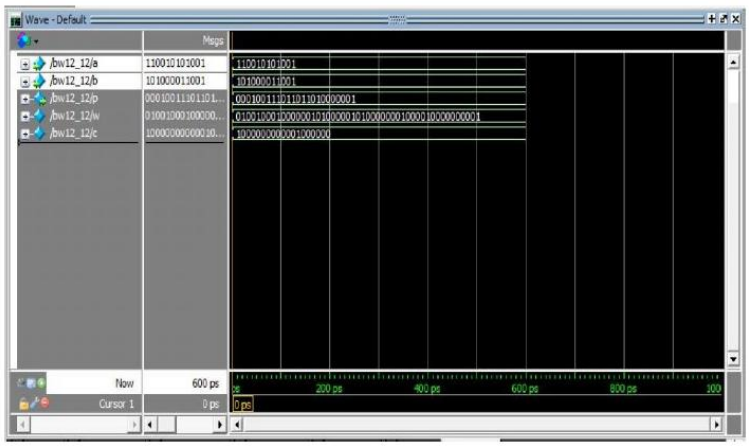

Figure 5: Simulation Result of Existed 12-Bit Baugh-Wooley Multiplier

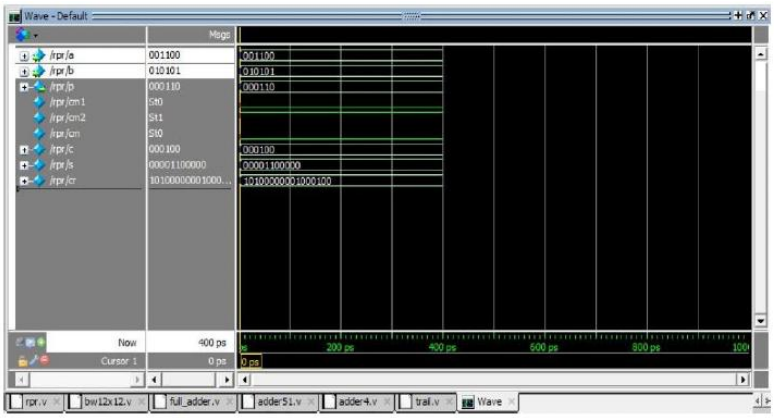

Figure 6: Simulation Result of Existed Fixed-Width RPR Block

CONCLUSION

In this article, a 12-bit low-error and location competent xed-width RPR-based ANT multiplier design was one time in ninety nm CMOS technology. The projected 12-bit Vedic multiplier with 8-bit constant width RPR circuit is executed in forty five nm CMOS technology. Under 0.6 V furnish voltage and 200-MHz operating frequency, the total energy consumption is 38.36 W. But for the 12-bit Vedic multiplier it consumes solely 24.013 W. Hence the power is efficaciously used and implemented

REFERENCES

[1] Curticapean, Florean, and Jarkko Niittylahti. "A hardware efficient direct digital frequency synthesizer." Electronics, Circuits and Systems, 2001. ICECS 2001. The 8th IEEE International Conference on. Vol. 1. IEEE, 2001.
[2] Hegde, Rajamohana, and Naresh R. Shanbhag. "Energy-efficient signal processing via algorithmic noise-tolerance." Low Power Electronics and Design, 1999. Proceedings. 1999 International Symposium on. IEEE, 1999.
[3] Wey, I-Chyn, Chien-Chang Peng, and Feng-Yu Liao. "Reliable low-power multiplier design using fixed-width replica redundancy block." IEEE Transactions on Very Large Scale Integration (VLSI) Systems 23.1 (2015): 78-87.
[4] Jou, Jer Min, Shiann Rong Kuang, and Ren Der Chen. "Design of low-error fixed-width multipliers for DSP applications." IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing 46.6 (1999): 836-842.
[5] Jon, Shyh-Jye, and Hui-Hsuan Wang. "Fixed-width multiplier for DSP application." Computer Design, 2000. Proceedings. 2000 International Conference on. IEEE, 2000.
[6] Kidambi, Sunder S., Fayez El-Guibaly, and Andreas Antoniou. "Area-efficient multipliers for digital signal processing applications." IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing 43.2 (1996): 90-95
[7] Kuang, S. R., and J. P. Wang. "Low-error configurable truncated multipliers for multiply-accumulate applications." Electronics letters 42.16 (2006): 1.
[8] Lim, Y. C. "Single-precision multiplier with reduced circuit complexity for signal processing applications." IEEE transactions on Computers 41.10 (1992): 1333-1336.
[9] Petra, Nicola, et al. "Truncated binary multipliers with variable correction and minimum mean square error." IEEE Transactions on Circuits and Systems I: Regular Papers 57.6 (2010): 1312-1325.
[10] Premananda, B. S., et al. "Design and implementation of 8-bit vedic multiplier." International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering 2.12 (2013): 5877-5882.
[11] Schulte, Michael J., and Earl E. Swartzlander. "Truncated multiplication with correction constant [for DSP]." VLSI Signal Processing, VI, 1993.,[Workshop on]. IEEE, 1993.

[12] Shim, Byonghyo, Srinivasa R. Sridhara, and Naresh R. Shanbhag. "Reliable low-power digital signal processing via reduced precision redundancy." IEEE Transactions on Very Large Scale Integration (VLSI) Systems 12.5 (2004): 497-510.
[13] Strollo, Antonio GM, Nicola Petra, and Davide De Caro. "Dual-tree error compensation for high performance fixed-width multipliers." IEEE Transactions on Circuits and Systems II: Express Briefs 52.8 (2005): 501-507.
[14] Pulimeno, Azzurra, Mariagrazia Graziano, and Gianluca Piccinini. "UDSM trends comparison: From technology roadmap to UltraSparc Niagara2." IEEE Transactions on Very Large Scale Integration (VLSI) Systems 20.7 (2012): 1341-1346.
[15] Gokila, D., and H. Mangalam. "Programmable Truncated Multiplier." Journal of Computational and Theoretical Nanoscience 13.8 (2016): 5046-5051.