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DESIGN OF A HIGH-PERFORMANCE FIR FILTER FOR AREA DELAY EFFECTIVE REALIZATION OF BOTH RECONFIGURABLE AND FIXED APPLICATIONS

M. Kavitha, Dr. Anjalai Bhardwaj

ABSTRACT

In this paper, it is possible to design block FIR (finite-impulse response) filter in transpose form for area-delay efficient realization of large order FIR filters. Generally, FIR filters are inherently pipelined and support multiple constant multiplications (MCM) technique which results in considerable computation saving. But, transpose form configuration does not directly support the block processing unlike direct form configuration. A flow graph for transpose form block FIR filter has derived with optimized register complexity based on an elaborated computational analysis of transpose form configuration of FIR filter. For reconfigurable applications, a general multiplier-based architecture has derived for the proposed transpose form block filter. The proposed design involves considerably less energy per sample (EPS) and less area delay product (ADP) than the existing block implementation of direct-form structure for medium or large filter lengths, while for the short-length filters, the block implementation of direct-form FIR structure has less EPS and less ADP than the proposed design.

KEYWORDS: FIR (Finite Impulse Response) filter, multiple constant multiplications (MCM), energy per sample (EPS), area delay product (ADP).

1. INTRODUCTION

FINITE impulse response (FIR) digital filter is one of the fundamental components in many digital signal processing (DSP) applications such as speech processing, loud speaker equalization, echo cancellation, adaptive noise cancellation, and various communication applications, including software-defined radio (SDR) and so on. In these, many applications require FIR filters of large order to meet the stringent frequency specifications. However, the number of multiplications and additions required for each filter output, increases linearly with the filter order. The output of an FIR filter having length N can be computed using the relation

$$y(n) = \sum_{i=0}^{N-1} h(i).x(n-i) \qquad (1)$$

Various researchers have suggested several designs for efficient realization of FIR filters (having fixed coefficients) using distributed arithmetic (DA) and multiple constant multiplication (MCM) methods. Generally, DA-based designs use lookup tables (LUTs) to store pre computed results to reduce the computational complexity and the MCM method on the other hand reduces the number of additions that are required for the realization of multiplications by common sub expression sharing, when a given input is multiplied with a set of constants. The MCM scheme is fit for the implementation of large order FIR filters with fixed coefficients. Because, it is more effective, when a common operand is multiplied with more number of constants. But, MCM blocks can be configured only in the transpose form configuration of FIR filters.

II. ARCHITECTURE OF FIR FILTER

The basic structure of an FIR filter is shown in Figure 1 (a). Using cut-set retiming, the pipelined version illustrated in Figure 1 (b) can be obtained and an inverted form FIR filter, which will be used

in FPGA implementations is depicted in Figure 1 (c). If the coefficient value is a sum of two powers-of-two, or an integer power-of-two, the multipliers can be replaced by shifters, as depicted in Figure 2. As the coefficients will be fixed for this category of filter, the coefficient values can be realized by appropriately routing the inputs to the full adders in the filter structure. That is, shifting the adder inputs k places to the left attains the same result as would a coefficient value of 2k .

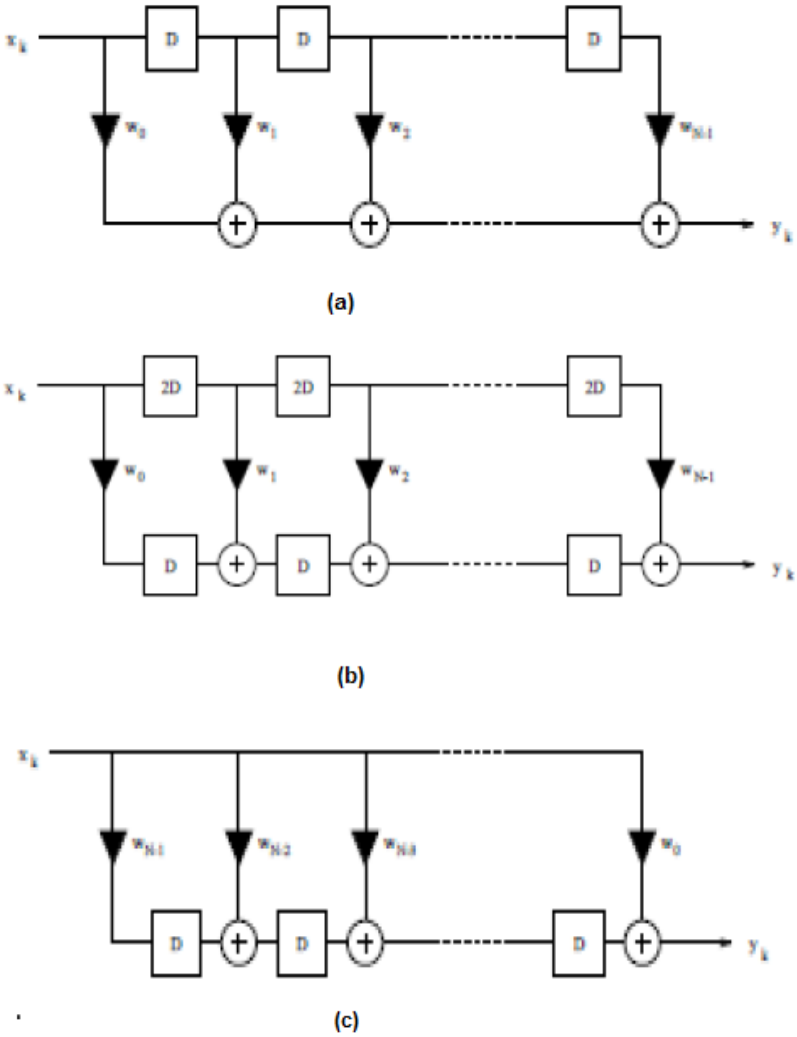


Figure1: FIR Filter Architecture
(a) canonical form, (b) pipelined, (c) inverted form.

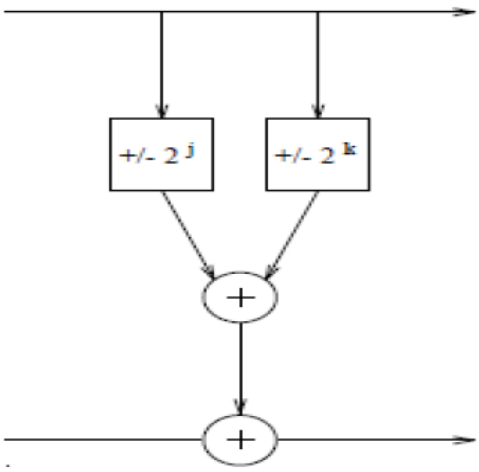


Figure 2: FIR Filter Tap Arithmetic Unit,
Coefficients with Two Powers-of-Two

Bit-level parallelism is exploited in order to get high sampling rates using conventional FPGAs or low cost CMOS processes. The overall filter architecture is shown in Figure 3, which consists of filter taps and final adder stage. The adder is essential to resolve the carries that are generated and propagated through the pipeline.

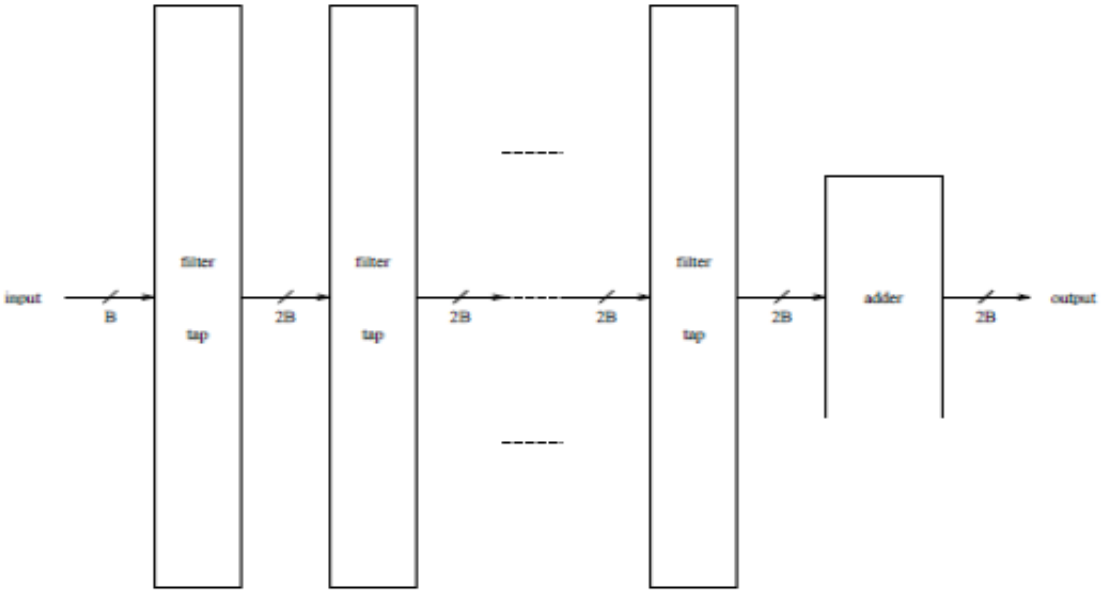


Figure 3: FIR Filter Architecture.

III. PROPOSED SYSTEM

In this section, we present a structure of block FIR filter for fixed filters using MCM scheme and also for reconfigurable applications. A. Proposed Structure for Transpose Form Block FIR Filter for Reconfigurable Applications The proposed structure for block FIR filter is [based on the recurrence relation of (2)] shown in Fig. 4 for the block size L = 4. It consists of one coefficient selection unit (CSU), one register unit (RU), M number of innerproduct units (IPUs), and one pipeline adder unit (PAU). The coefficients of all the filters to be used for the reconfigurable application are stored in CSU. It is designed making use of N ROM LUTs, such that filter coefficients of any particular channel filter are obtained in one clock cycle, where N is the filter length. The RU receives xk during the kth cycle and yields L rows of S 0 k in parallel. L rows of S 0 k are transferred to M IPUs of the proposed structure. In addition to the L rows of S 0 k, the M IPUs receive M shortweight vectors from the CSU such that during the kth cycle, the (m + 1)th IPU receives the weight vector cM−m−1 from the CSU and L rows of S 0 k form the RU. Each IPU carries out matrix-vector product of S 0 k with the short-weight vector cm, and computes a block of L partial filter outputs (r m k).

Therefore, each IPU executes L inner-product computations of L rows of S 0 k with a common weight vector cm. The (l+1)th inner-product cell (IPC) which is a part of IPU incurs the (l+1)th row of S 0 k and the coefficient vector cm, and computes a partial result of inner product r(kL −l), for $0 \leq l \leq$ L-1. All the M IPUs work in parallel and produce M blocks of result (r m k). In PAU, these partial inner products are added to obtain a block of L filter outputs. In each cycle, the intended structure receives a block of L inputs and yields a block of L filter outputs, where the duration of each cycle is T = TM + TA +TFA log2 L, TM is one multiplier delay, TA is one adder delay, and TFA is one full-adder delay.

$$\mathbf{Y}(z) = \mathbf{S}^0(z)[(z^{-1}(\ldots(z^{-1}(z^{-1}\,\mathbf{c}_{M\text{-}1} + \mathbf{c}_{M-2}) + \mathbf{c}_{M-3}) + \ldots) + \mathbf{c}_1) + \mathbf{c}_0] \qquad (2)$$

where S 0 (z) and Y(z) are the z-domain representation of S 0 k and yk , respectively.

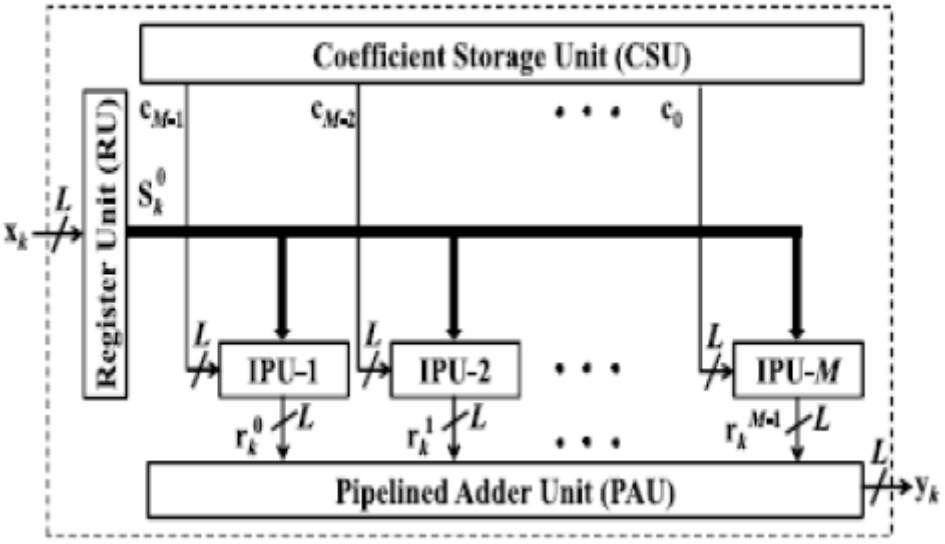


Figure 4: Proposed structure for block FIR filter

B. MCM-Based Implementation of Fixed-Coefficient FIR Filter

For fixed-coefficient implementation, the CSU of Fig. 4 is not required, since the structure is to be tailored for only one given filter. Similarly, IPUs are also not required. The multiplications are required to be mapped to the MCM units for a lowcomplexity realization. We show in the following that the proposed formulation for MCM-based implementation of block FIR filter makes use of the symmetry in input matrix S 0 k to perform horizontal and vertical common subexpression elimination and to reduce the number of shift-add operations in the MCM blocks. The recurrence relation of (2) can be written as

$$\mathbf{Y}(z) = z^{-1} \ldots z^{-1}(z^{-1}\mathbf{r}_{M-1} + \mathbf{r}_{M-2} + \mathbf{r}_{M-3}) + \ldots + \mathbf{r}_1 + \mathbf{r}_0 \qquad (3)$$

The M intermediate data vectors rm, for $0 \le m \le M-1$ can be computed using the relation

$$\mathbf{R} = \mathbf{S}^0{}_k.\mathbf{C} \qquad (4)$$

where R and C are defined as

$$\mathbf{R} = [\, \mathbf{r}^T{}_0 \;\; \mathbf{r}^T{}_1 \;\; \ldots \;\; \mathbf{r}^T{}_{M-1} \,] \qquad (5)$$

$$\mathbf{C} = [\, \mathbf{c}^T{}_0 \;\; \mathbf{c}^T{}_1 \;\; \ldots \;\; \mathbf{c}^T{}_{M-1} \,] \qquad (6)$$

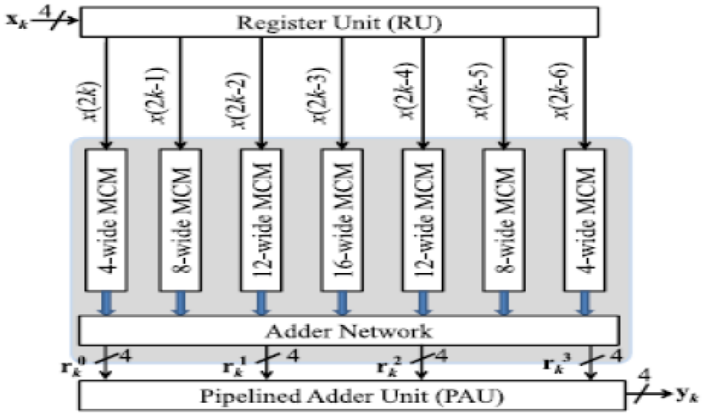


Figure 5: Proposed MCM-based structure for fixed FIR filter of block size L = 4 and filter length N = 16.

IV. RESULT

Simulation Result:

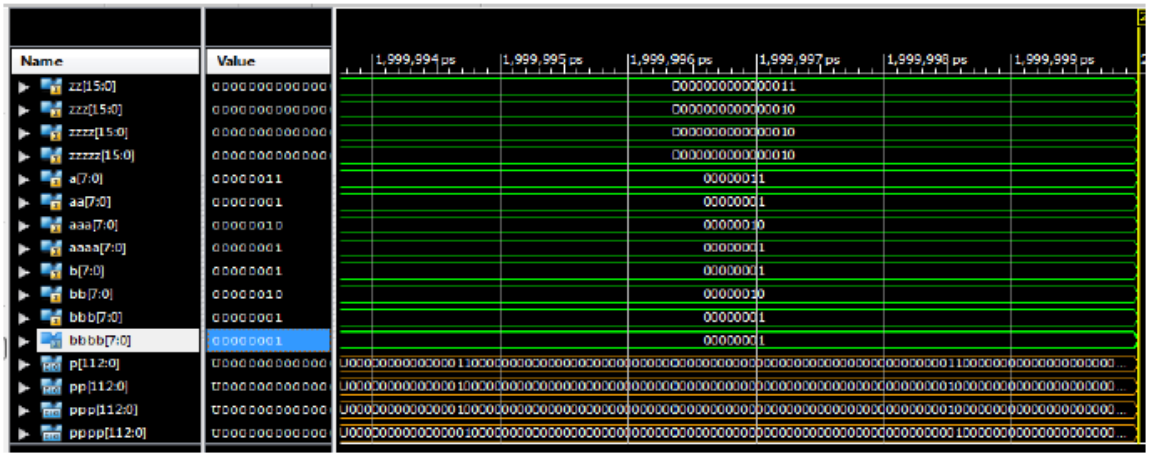


Figure 6: Input

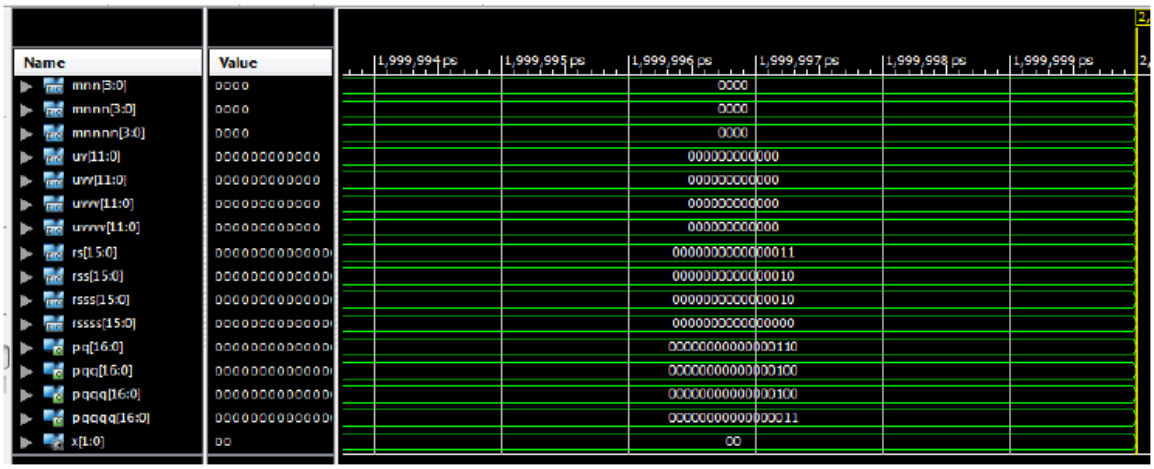
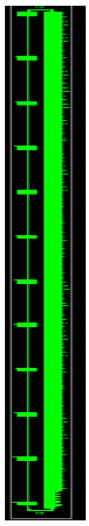


Figure 7: Output

RTL Schematic:



V. CONCLUSION

In this report, we have examined the possibility of realization of block FIR filters in transpose form configuration for area delay effective realization of both reconfigurable and fixed applications. For transpose form block FIR filter, a generalized block formulation is presented and based on that we have developed transpose form block filter for reconfigurable applications. We have represented a

strategy to recognize the MCM blocks for horizontal and vertical sub expression elimination in the proposed block FIR filter for fixed coefficients to decrease the computational complexity.

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