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Optimal Topology in Multilevel Inverter for Power Quality Improvement using PWM Strategies

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Abstract
The general function of a multilevel converter is to synthesize a desired output voltage from several levels of dc voltage as inputs. In order to increase the steps in the output voltage, a new topology is recommended in this paper, Various topologies of multilevel inverter provides several advantages including Power voltage stress, higher efficiency, lower EMI, better waveforms, low switching losses and improved THD. This paper proposes the simulation of novel algorithms for Cascaded H-Bridge Cell Multilevel Inverter to improve power quality by optimizing its structure. The optimization of structures is achieved by reducing the number of power semiconductor switches in the inverter. This is achieved with the help of mathematical equations which are obtained from the structure of the inverter. To validate the proposed algorithms the simulation results are compared with conventional methods.

Keywords - Cascaded H-Bridge (CHB) Multilevel Inverter (MLI), Pulse Width Modulation (PWM), Total Harmonic Distortion(THD)

I) INTRODUCTION

The general function of a multilevel converter is to synthesize a desired output voltage from several levels of dc voltages as inputs[1]. In order to increase the steps in the output voltage, a new topology is proposed in the reference [2], which benefits from a series connection of sub-multilevel converters. In the procedure described in this reference, despite all the advantages, it is not possible to produce all the steps (odd and even) in the output. In addition, for producing an output voltage with a constant number of steps, there are different configurations with a different number of components [2]-[3]. In this chapter, the optimal structures for this topology are investigated for various objectives such as minimum number of switches and dc voltage sources and minimum standing voltage on the switches for producing the maximum output voltage steps. Two new algorithms
for determining the dc voltage sources magnitude have been proposed. A new general cascaded multilevel inverter using developed H-bridges is proposed. The proposed topology requires a lesser number of dc voltage sources and power switches and consists of lower blocking voltage on switches, which results in decreased complexity and total cost of the inverter. A new single-phase H-bridge multilevel inverter (MLI) topology constructed using auxiliary reverse-connected voltage sources along with a hybrid pulse width modulation (PWM) strategy is proposed [4]-[6], to extract a variable frequency variable amplitude output voltage. It involves the use of reduced number of switching devices for a specific

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number of output voltage levels in comparison with conventional MLIs. There are different methods for different voltage sources in asymmetric methods have also deployed [14]-[17].

II) OPTIMAL STRUCTURES FOR PROPOSED MULTILEVEL INVERTER

The basic unit of multilevel converter consists of a dc voltage sources (with a voltage equal to Vdc) with four unidirectional switches. There are several arrangements that can be used to create such a unidirectional switch. The basic unit of our proposed topology is shown below. The basic unit in series can increase the possible values of Vo. If n dc voltage sources are used in the extended unit, then
the number of output voltage steps (Nsteps) and switches (Nswitch) are given by the following equations, respectively.

$N_{step} = n(n + 1) + 1$ (1)

$N_{switch} = 2(n + 1)$ (2)

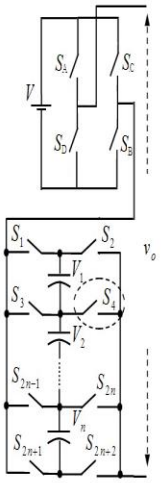

Fig -1 Proposed Topology Diagram

The presented extended unit requires bidirectional switches with the ability to block voltage and conducting current in both directions. In this chapter, the common emitter configuration has been used. The advantage of this configuration is that each bidirectional switch requires a gate driver circuit. It is important to note that only two switches for each extended unit turn on in the different modes of converter operation. The extended basic units in series can increase the possible values of Vo. In this case, the number of output voltage steps and switches are given by the following equations, respectively:

$$N_{step} = \prod_{i=1}^{k}[n_i(n_i + 1) + 1] \quad (3)$$

$$N_{switch} = \prod_{i=1}^{k}[2(n_i + 1)] \quad (4)$$

The output voltage of the converter can be calculated as follows:

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$$V_O(t) = \sum_{j=1}^{k} v_{0,j} \qquad (5)$$

and the peak value of the output voltage is calculated as follows:

$$V_{0,\max} = \sum_{j=1}^{k} \sum_{i=1}^{n_j} v_{i,j} \qquad (6)$$

Although this topology requires multiple dc sources, in some systems they may be available through renewable energy sources such as photovoltaic panels or fuel cells or with energy storage devices such as capacitors or batteries. When an ac voltage is already available, multiple dc sources can be generated using isolated transformers and rectifiers.

A)Proposed Algorithm 1

In this algorithm it is proposed that the values for all of the dc voltage sources for generating odd and even steps can be calculated using the following relationships:

First stage:

$V_{1,1} = V_{dc}$ (7)

$V_{j,1} = 2V_{dc}$ for j = 2; 3; _ _ _ ; n_1 (8)

Second stage:

$$V_{1,2} = V_{dc} + 2\sum_{j=1}^{n_1} V_{j,1} = (4n_1 - 1)V_{dc} \qquad (9)$$

$V_{j,2} = 2(4n_1\text{-}1)V_{dc}$ for j = 2; 3; _ _ _ ; n_2 (10)

M^{th} stage:

$$V_{1,m} = V_{dc} + 2(\sum_{i=1}^{m-1} \sum_{j=1}^{n_i} V_{j,1}{}_{dc} \qquad (11)$$

$V_{j,m} = 2V_{1,m}$ for j = 2; 3; _ _ _ ; n_m: (12)

One of the advantages of this algorithm when compare to the algorithm recommended in [1] is the ability to produce all of the steps at the output voltage. A reduction in the variety of the values of the dc voltage sources is another advantage of this algorithm. The disadvantage of this algorithm is that two or more switching states produce the same output voltage. These states are called redundant states. Obviously this kind of redundancy is strictly related to the hardware architecture of the converter and the values of the dc voltage sources. In the proposed algorithm, the number of output voltage steps is obtained as follows:

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$$N_{step} = \prod_{i=1}^{k}[4n_i - 1)] \qquad (13)$$

B) Proposed Algorithm 2

For a greater reduction in the variety of the values of the dc voltage sources, another new algorithm is proposed as follows:

First stage:

$V_{j,1} = V_{dc}$ for j = 1; 2; 3; _ _ _ ; n_1 (14)

Second Stage:

$$V_{j,2} = V_{dc} + 2\sum_{i=1}^{n_1} V_{i,1} = (2n_1 + 1)V_{dc}$$

for j=1,2,…,n_2 (15)

M[th] stage:

$$V_{j,m} = V_{dc} + 2(\sum_{i=1}^{m-1}\sum_{l=1}^{n_i} V_{j,l}) \text{ for j=1,2,…,} n_m \qquad (16)$$

This algorithm produces redundant states. In this algorithm, the number of output voltage steps is given as follows:

$$N_{step} = \prod_{i=1}^{k}[2n_i + 1)] \qquad (17)$$

Considering (13) and (17), it is clear that the first proposed algorithm can generate a larger number of steps. In other words, the number of redundant states in the first algorithm is less than with the second algorithm. In contrast, in the second algorithm, the variety of the values of the dc voltage sources is less than with the first algorithm.

III) SIMULINK MODEL OF PROPOSED FIFTEEN LEVEL AND TWENTY ONE LEVEL INVERTER

The MATLAB/SIMULINK model of the proposed topology is shown in Fig..2. Optimal Structures 1 and 2 are separately developed in the SIMULINK environment. The parameters selected for components in optimal structure 1 and 2 are given in Table 1. In the output voltage, 21 levels are obtained in proposed algorithm 1 and 15 levels are obtained in proposed algorithm 2 and the results are compared.

PARAMETERS OF THE SYSTEM – TABLE 1

Parameters	Values
OPTIMAL STRUCTURE 1	

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MOSFETs : 16	
FET resistance	0.1Ω
Snubber resistance	100000Ω
Snubber capacitance	inf

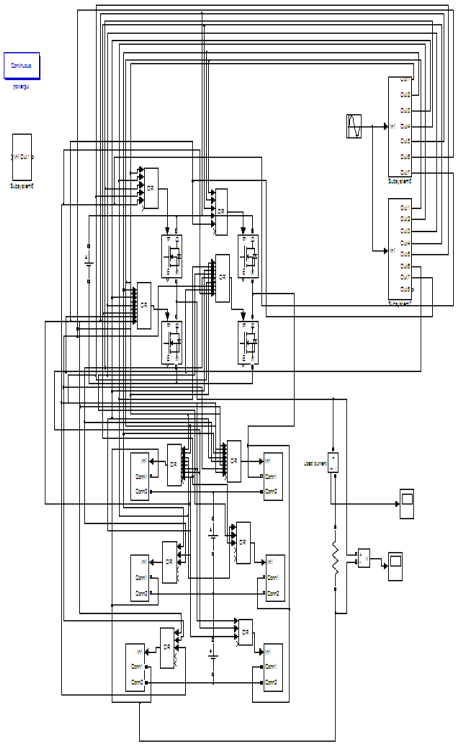

Figure – 2 Simulink Model of Proposed Topology

IV) SIMULATION RESULTS

A) OUTPUT WAVEFORM OF SEVEN LEVEL CHBMLI

The output voltage waveform for the existing topology with PWM technique is shown in the Fig.3. The voltage waveform has seven levels with each level contributing 100 volts and output is obtained across the resistive load of 100 ohms.

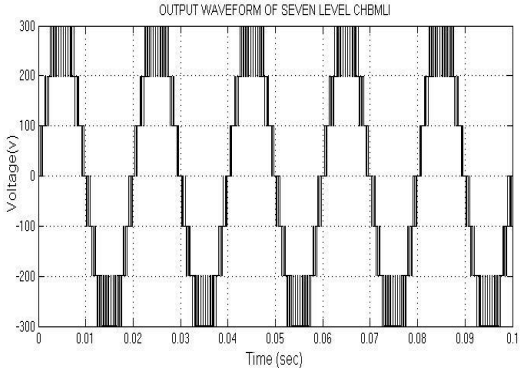

Fig -3Output waveform of seven level inverter

B) THD SPECTRUM OF SEVEN LEVEL CHBMLI

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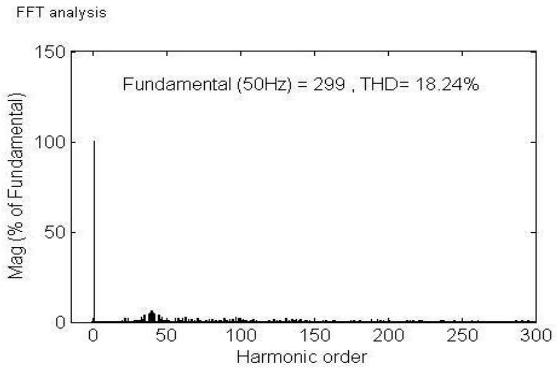

Fig -4 THD for output waveform of seven level inverter

The above diagram shows the fast fourier transform analysis of the seven level MLI output. The total harmonic distortion was obtained to be 18.24% and the fundamental peak voltage was obtained as 299 volts at a frequency of 50 Hz.

C) OUTPUT WAVEFORM OF ELEVEN LEVEL MLI

The output voltage waveform for the exiting topology with PWM technique is shown in the Fig.5. The voltage waveform has seven levels with each level contributing 100 volts and output is obtained across the resistive load of 100 ohms.

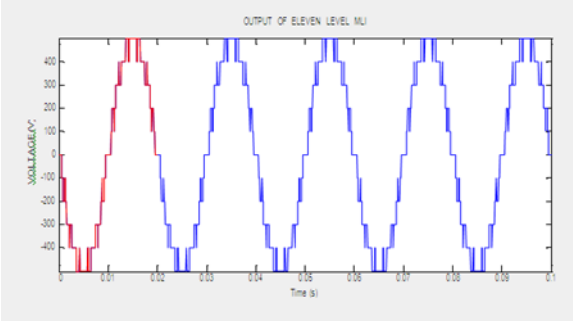

Fig.5. Output waveform of Eleven Level MLI

D) THD OF ELEVEN LEVEL INVERTER

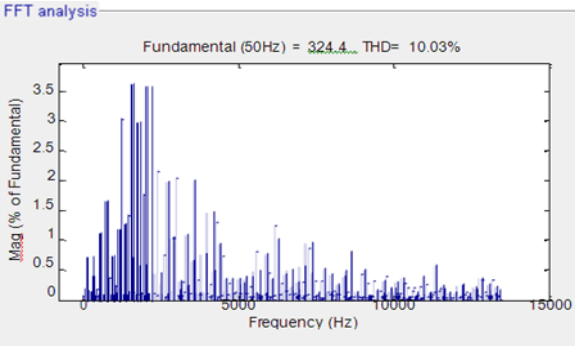

Fig.6. Total Harmonic Distortion of Eleven Level Inverter

The above figure 6 shows the Fast Fourier Transform Analysis of the eleven level MLI output. The total harmonic distortion is obtained to be 10.03% and the fundamental peak voltage is found to be 324.4 V at a frequency of 50Hz

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E) OUTPUT WAVEFORM OF FIFTEEN LEVEL MLI

The output voltage waveform for the proposed topology with PWM technique is shown in Fig.7. The voltage waveform has fifteen levels with each level contributing 10 Volts and output is obtained across the RL loads.

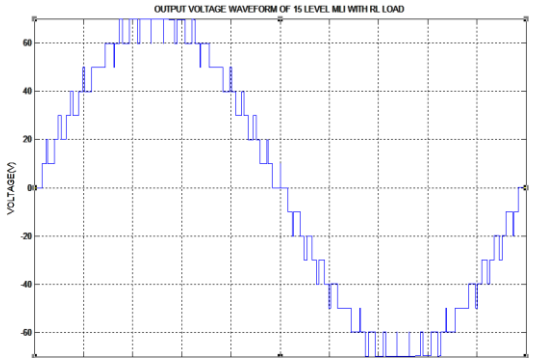


Fig.7. Output waveform of Fifteen Level MLI

F) TOTAL HARMONIC DISTORTION OF FIFTEEN LEVEL INVERTER

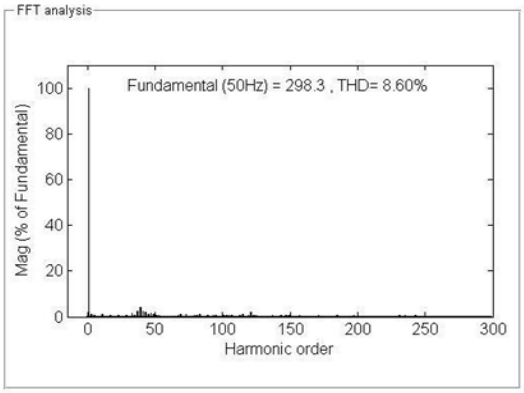
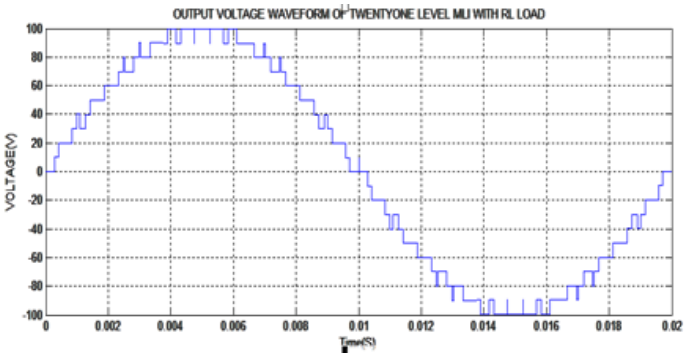


Fig.8. Total harmonic distortion of Fifteen level inverter

The above diagram shows the fast fourier transform analysis of the fifteen level MLI output. The total harmonic distortion was obtained to be 8.60% and the fundamental peak voltage was obtained as 298.3 volts at a frequency of 50 Hz.

G) OUTPUT WAVEFORM OF TWENTY ONE LEVEL MLI

The output voltage and current waveform for the proposed topology with PWM technique is shown in the Fig.9. The voltage waveform has twenty one levels with each level contributing 10 Volts and output is obtained across the RL loads.



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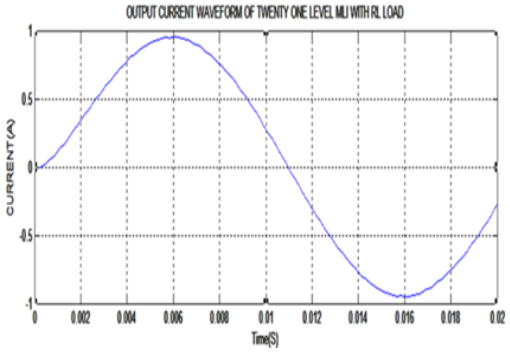

Fig.9 Output Voltage and Current waveform of twenty one level MLI

H) TOTAL HARMONIC DISTORTION OF TWENTY ONE LEVEL INVERTER

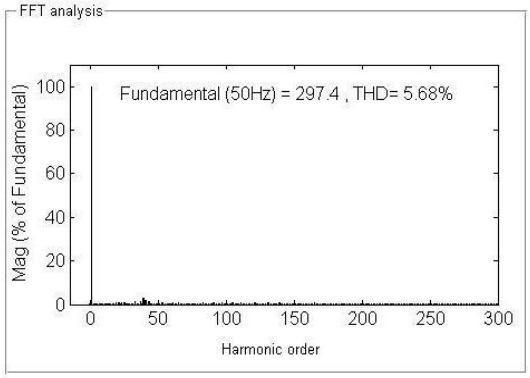

Fig.10. Total harmonic distortion of twenty one level inverter

The above diagram shows the fast fourier transform analysis of the fifteen level MLI output. The total harmonic distortion was obtained to be 5.68% and the fundamental peak voltage was obtained as 297.4 volts at a frequency of 50 Hz.

TABLE II

COMPARISON OF DIFFERENT LEVELS OF MLI

Modulation Index	Output Voltage (v)	Total Harmonic Distortion %		
		7 Level	15 Level	21 Level
1.0	300	18.24	8.60	5.68
0.9		22.40	8.79	6.80
0.8		24.34	10.07	6.81
0.7		25.20	11.55	8.62
0.65		28.67	12.94	8.34

V) CONCLUSION

In this paper, two new algorithms for the determination of the magnitudes of dc voltage sources have been proposed. These algorithms can provide all steps (odd and even). It was shown that the structure consisting of units with two dc voltage sources is the best case to keep the minimum number of switches for a certain number of voltage steps. In addition, it

was proven that the topology, consisting of units with one dc voltage source, is the optimal structure for minimizing the standing voltage on the switches, and that it minimizes the number of dc voltage sources. The two control algorithms proposed for the MLI topology presented in this paper prove that with the same number of switches number of levels in the output voltage can be increased so as to reduce the THD without any increase in the control circuit complexity. The resulting output AC voltage swings with seven, fifteen and twenty one levels prove that the control methods for the proposed structure result in a staircase like waveform which is nearly sinusoidal, even without passing through any filter.

REFERENCES

[1] Muhammad H. Rashid, " Power Electronics circuits, devices, and applications", Pearson education Inc,2004.
[2] E. Babaei, S. H. Hosseini, G. B. Gharehpetian, M. Tarafdar Haque and M. Sabahi, "Reduction of dc voltage sources and switches in asymmetrical multilevel converters using a novel topology," Elsevier Journal of Electric Power System Research, Vol. 77, pp. 1073-1085, Jun. 2007.
[3] E. Babaei, S. Alilu, and S. Laali, "A new general topology for cascaded multilevel inverters with reduced number of components based on developed H-bridge," IEEE Trans. Ind. Electron., vol. 61, pp. 3932-3939, Aug. 2014.
[4] Leopoldo G Franquelo, Jose Rodriguez, Jose I leon, Samir Kouro, Raman Portillo, Maria A.M Prats, "The age of multilevel converters arrives", IEEE industrial electronics Magazine, June 2008.
[5] Jose Rodriguez, Jih-Sheng lai, and Fang Zheng, ", Multi level inverters: A survey of topologies, Controls and applications", IEEE industrial electronics Magazine, vol.49,August 2002.
[6] Gui-Jia Su, "Multilevel DC link Inverter", IEEE industrial applications, vol.41, May/June 2005.
[7] Ramkumar. S, Kamaraj. V, Thamizharasan. S & Jeevananthan. S, "A new series parallel switched multilevel dc-link inverter topology", International Journal of Electrical Power and Energy Systems, vol. 36, pp. 93-99, 2012
[8] Baskaran, J., Ramkumar, S. and Jeevananthan, S., "Cross switched multilevel inverter using auxiliary reverse-connected voltage sources", IET Power Electronics, Vol. 7, pp. 1519-1526, 2014.
[9] Thamizharasan. S, Baskaran.J, Ramkumar. S and Jeevananthan, S., "A new dual bridge multilevel dc-link inverter topology", International Journal of Electrical Power and Energy Systems, Vol. 45, pp. 376-383, 2013.
[10] Domingo A Ruiz-Caballero, Reynaldo M Ramos-Astudillo, Samir ahmad Mussa, Member, marcelo Lobo Heldwein,, " Symmetrical Hybrid multilevel DC-AC converters with reduced number of insulated DC supplies", IEEE industrial electronics Magazine, vol.57,July 2010.
[11] Youhei Hinago, and Hirotaka Koizumi, "Single phase multi level inverter using switched Series/parallel DC voltage sources", IEEE industrial electronics Magazine, vol.5,August 2010.
[12] Martin Veenstra, and Alfred Rufer, "Control of a hybrid asymmetric multilevel inverter for competitive medium-voltage industrial drives", IEEE industrial applications, vol.41,March/April 2005.

[13] Leon M. Tolbert, John Chiasson, Keith McKenzie, Zhong Du, "Elimination of harmonics in a multilevel converter with non equal DC sources", IEEE transaction on Industry applications, Vol.41, 2005.
[14] M.R.Banaei, E, Salary, S Najafi Ravadanegh, "Stacked Multicell Cascaded transformer Multilevel Inverter," Proc. Power Electron.Spec.Conf., pp.422-427, 2012.
[15] Y.S.Lai and F. S. Shyu, "Topology for hybrid multilevel inverter," IEEE Proc. Electr. Power Applicat., vol. 149, pp. 449-458, 2002.
[16] E.Babaei, S.H. Hosseini, G.B. Gharehpetian, M. Tarafdar Haque and M.Sabahi, "Reduction of dc voltage sources and switches in asymmetrical multilevel converters using a novel topology," Electric Power Systems Research, pp. 1073-1085, 2007
[17] E.Babaei, "Optimal Topologies for Cascaded Sub-Multilevel Converters," Journal of Power Electronics, vol.10, no. 3, pp. 251-261, May 2010.